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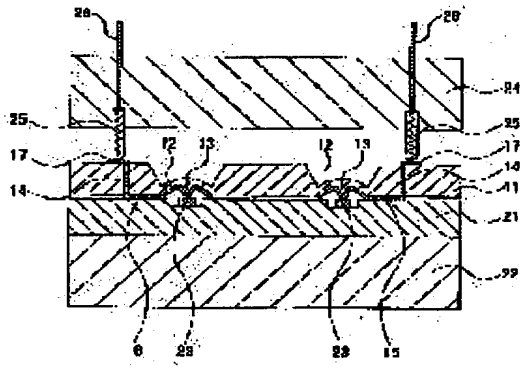
(71)Applicant : HITACHI LTD
(72)Inventor : HOSOGANE ATSUSHI
KANAMARU MASATOSHI
KONO RYUJI
ENDO KIJU
ARIGA AKIHIKO
BAN NAOTO
AOKI HIDEYUKI

(54) MANUFACTURE OF SEMICONDUCTOR INSPECTION DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To collectively inspect the electrode pads having a large area of a wafer to be inspected by forming such a beam or diaphragm structure that probes are changed by pressing forces in a substrate on which the probes are formed and pressing or fixing the wafer in which the electrode pads are formed.
SOLUTION: A plurality of probes 13 is formed in an inspection wafer 11 by forming a coating film on the surface of a silicon substrate and, after the film is patterned by photolithography, a plurality of probes 13 by etching. Then, after the coating film is removed, diaphragms 12 are formed at every probe 13 in the same process. In the same process, in addition, through holes 14 are formed correspondingly to the probes 13 and wiring 16 is formed from the probes 13 to secondary-side electrode pads 17 through the through holes 14. The electrode pads 17 are connected to POGO pins 25 and the wafer 11 fixed to a pressing mechanism supporting substrate 23 is pressed against a wafer 21 to be inspected on a wafer fixing stage 22. Therefore, the probes 13 can evenly inspect the primary-side electrode pads 23 of the wafer 21 for electric characteristics, because the probes 13 come into contact with the electrodes pads 23, resulting in the deformation of the diaphragms 12, and a fixed load is applied between the probes 13 and electrode pads 23.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] Two or more probes formed in the field of one side of a silicon substrate Wiring which flows through two or more electrodes formed in the field of the other side of said silicon substrate, and said two or more probes and said two or more electrodes electrically The process which is the manufacture approach of semi-conductor test equipment equipped with the above, forms a coat on the surface of a silicon substrate, and forms the shape of a pyramid, and two or more conic probes by etching after patterning by the photolithography, The process which forms a coat on the surface of a silicon substrate again, and forms a beam or a diaphragm for said every probe by etching after patterning by the photolithography after removing a coat, The process which forms a coat on the surface of a silicon substrate again, and forms a through tube by etching after patterning by the photolithography after removing a coat corresponding to said probe, It is characterized by performing the process which forms an insulating coat on the surface of a silicon substrate again, forms a metal coat in the front face of said insulating coat after removing a coat, and forms wiring by etching after patterning by the photolithography.
[Claim 2] The manufacture approach of the semi-conductor test equipment characterized by having a flat part at the tip of a probe in claim 1.
[Claim 3] The manufacture approach of the semi-conductor test equipment characterized by the structure of a beam being a doubly-supported beam in claim 1.
[Claim 4] The probe formed in one principal plane of a silicon substrate The electrode formed in the field opposite to one principal plane of said silicon substrate A means to flow through said probe and said electrode electrically It is semi-conductor test equipment equipped with the above, and is characterized by performing the connection with the inspection wafer by the press substrate, and press using the number of electrodes of a **-ed wafer, the same number, or the POGO pin beyond it.
[Claim 5] Semi-conductor test equipment characterized by performing the connection with the inspection wafer by the press substrate, and press using the number of electrodes of a **-ed wafer, the same number, or the solder ball beyond it in claim 4.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the inspection approach of of the semiconductor device or semiconductor device formed on the wafer, especially relates to the test equipment for electrical-characteristics measurement in semi-conductor production processes, such as probing inspection and burn-in inspection.
[0002]
[Description of the Prior Art] It is divided roughly into a last process until it forms a circuit in a silicon wafer front face, and a back process until it separates this silicon wafer for the chip according to individual and closes with resin, a ceramic, etc. in semiconductor devices, such as IC (integrated circuit) and LSI (large-scale integrated circuit). In these semiconductor devices, electrical-characteristics inspection of each circuit is conducted in the predetermined phase in a last process, and the judgment of an excellent article and a defective is performed per chip. It can classify to that the above-mentioned electrical-characteristics inspection is thermal in probing inspection which distinguishes the quality of the flow between each circuit, and an about 150-degree C elevated temperature, and burn-in inspection which carries out acceleration sorting of the defect by giving electrical stress to a circuit.
[0003] probing inspection and burn-in inspection -- the fundamental connecting means of a **-ed wafer and external check system -- abbreviation -- it is the same. That is, the approach of pressing a conductive detailed probe mechanically separately to the electrode pad of each aluminium alloy with an angle [dozens thru/or hundreds of micrometer angle] by which patterning was carried out, and a thickness of about 1 micrometer, or other alloys in dozens thru/or hundreds of micrometer pitch is adopted on the **-ed wafer.
[0004] Conventionally, the structure of the used probe is shown in drawing 13 and drawing 14 .
[0005] Each probe 141 is mainly the thin needle of 10 micrometers of tip parameters, and 10mm of die-length numbers in the product made from a tungsten, and it is fixed or fabricated in drawing 13 by the substrate 142 and the insulating fixture 143 so that a tip location may correspond to each electrode pad of a **-ed wafer.
[0006] the probe 151 of each [drawing 14] -- mainly -- plating -- accumulating -- it is the metal projection of the shape of a pyramid which formed the metal projection of the shape of a fabricated semi-sphere, or the anisotropic etching hole of a silicon substrate as a plating mold etc., and this aggregate is formed in the front face of the organic thin films 152, such as polyimide.
[0007] Moreover, JP,6-123746,A, JP,7-7052,A and JP,8-50146,A, and JP,9-243663,A are exhibited as a means to solve the trouble of the two above-mentioned examples mentioned later.
[0008] In JP,6-123746,A, slitting was put into the card in which elastic deformation is possible, two or more probe needles in which elastic deformation is possible were formed in homogeneity, and two or more contact which can contact the electrode of a semiconductor device is prepared according to the individual at each point of two or more of these probe needles.
[0009] moreover -- JP,7-7052,A -- single crystal silicon, silicon oxide, silicon nitride, polish recon, or a metal layer -- at least -- much more -- since -- it considers as the becoming cantilever structure, and this cantilever structure is further held by the insulating substrate in which the metallic film for a flow was formed on that front face and in which the flow circuit pattern was formed, and it is considering as the probe for electrical property measurement.
[0010] On the other hand, in JP,9-243663,A, a silicon substrate is processed in the shape of a diaphragm, and the probe for filling up with an elastomer the diaphragm section of the structure in which two or more contact probes were formed to the contact side, and measuring an electrical property is formed.
[0011]
[Problem(s) to be Solved by the Invention] There was a trouble as shown below by the inspection approach of a semiconductor device which was stated with the above and the conventional technique.
[0012] It was difficult to need great time amount for positioning and fixing each probe with high precision with the probe structure shown in drawing 13 , and to mass-produce the probe structure cheaply. Moreover, since many fields for positioning and fixing each probe were needed, it is difficult to arrange many probes by the inside of a substrate, and the number of electrode pads or the number of chips which can be inspected at once was restricted. Furthermore, since each probe length was as large as about dozens of mm, the regulation capacity in each probe was large, and parenchyma was impossible for inspection of a high-speed device about 100MHz or more.
[0013] Moreover, in order to destroy the insulating natural oxidation film with which the radius of curvature of each end of the probe was large with the film, and was formed in the electrode pad front face of a **-ed wafer Since the actuation which carries out the scribe (marking-off) of a big press load and the electrode pad front face is needed, Wear of the end of the probe was brought forward, and there was a problem with which the dust of the electrode pad generated by about [that the life (count of durable inspection) of a probe was short] and the scribe pollutes the environment in semiconductor device manufacture.
[0014] Moreover, since a probe was arranged in a detailed pitch on organic thin film front faces, such as polyimide, in the probe structure shown in drawing 14 corresponding to the electrode pad of a **-ed wafer, it was difficult to absorb independently dispersion in the distance of the probe produced by the curvature of a **-ed wafer, or dispersion of the height of a probe, and a corresponding electrode pad. Moreover, since organic thin films, such as polyimide with which coefficient of linear expansion differs from a **-ed wafer greatly, were used as the base material, by burn-in inspection conducted in an about 150-degree C elevated temperature, the big

differential thermal expansion arose between **-ed wafers, and there was a case where the location gap with an electrode pad and a probe arose, with the probe in the location distant from the core.
[0015] Moreover, in JP,6-123746,A, since a card consisted of synthetic resin or a metal, formation of two or more probe needles in which elastic deformation is possible was difficult for probe arrangement in the detailed pitch corresponding to the electrode pad location of a **-ed wafer, i.e., each.
[0016] In JP,7-7052,A, in order to join anew each cantilever probe formed with the silicon system base material to an insulating-substrate front face different from it, the manufacture yield fell, and there was a problem of an ununiformity in the height of the probe of further each.
[0017] Although it is indicated by JP,9-243663,A that the diaphragm section formed in the silicon substrate along with distortion of a **-ed wafer deforms using an elastomer (elastic material), by this method, dispersion in the thickness of a diaphragm is not taken into consideration, and when a diaphragm with dispersion in a wave or thickness is made to deform, control of the height of a contact probe cannot be performed. Therefore, since the depth direction of the pad for electrical-characteristics measurement of a **-ed wafer is uncontrollable, when thrust is insufficient, the part which does not contact the pad section for electrical-characteristics measurement of a **-ed wafer comes out. Moreover, when thrust was put too much, it sank into the pad section for electrical-characteristics measurement of a **-ed wafer deeply, and there was a problem which destroys a **-ed wafer.
[0018] Moreover, since wiring for the electrical installation of the tip of a probe and external check system is formed in the same front face as the probe forming face in a substrate for which the above-mentioned probe structure, It does not obtain. all external connection terminals -- the near periphery of a base material -- concentrating -- not forming -- It was difficult to limit the field of this external connection terminal which can be formed, and to connect many probes with the exterior electrically, for example, large field coincidence inspection of inspecting all the electrode pads of a **-ed wafer collectively was difficult.
[0019] The purpose of this invention solves many troubles described until now, enables large field coincidence inspection which says that all the electrode pads of a **-ed wafer carry out package inspection in electrical-characteristics inspection of a semiconductor device, raises the manufacture yield by it, reduces a manufacturing cost, is cheap and is to obtain the semiconductor device which has high-reliability.
[0020]
[Means for Solving the Problem] It can attain by establishing the device which presses the probe or the probe periphery of the device which presses or fixes the **-ed wafer with which a semiconductor device and test equipment were contacted directly, the beam structure or the diaphragm structure where of a probe could change with thrust to the substrate with which the probe was formed in the approach of inspecting a semiconductor device was formed, connecting electrically, and the electrode pad of a checking semiconductor device was formed in order to attain the above-mentioned purpose, or said substrate. Moreover, it is good to use silicon for the substrate with which the above-mentioned probe was formed, to constitute a probe from silicon, metals, or those composites, and to use the structure currently wired at the rear-face side of a probe formation substrate with wiring using a conductive ingredient through an insulating material. Moreover, it is possible by having the flat-surface section in the point of this probe to form probe height in homogeneity with high precision moreover.
[0021] The structure which the structure of the probe formed in the doubly-supported beam which became independent separately was desirable, formed the probe in the longitudinal plane of symmetry, and formed the beam in the fylfot type configuration for the perimeter may be used. Anisotropic etching or dry etching is used for processing of the structure including these beams. By using ICP-RIE (InductivelyCoupled Plasma-Reactive Ion Etching) equipment for the above-mentioned dry etching, it is possible to form spacing of a beam and a beam narrowly, and it can respond also to ** pitch-ization of a device.
[0022] Wiring uses anisotropic etching or dry etching for an inspection wafer, makes this substrate penetrate and uses the approach of wiring electrically the probe forming face and rear face of this substrate using a spatter, vacuum evaporationo, or plating. Moreover, the through tube of an inspection wafer has the good method formed using dry etching. Furthermore, the semiconductor device or electronic parts inspected using above-mentioned structure and an above-mentioned approach is very cheap, and can be offered.
[0023]
[Embodiment of the Invention] Hereafter, the example of this invention is explained using a drawing. Drawing 1 is the sectional view showing the 1 actual example of the structure of the inspection wafer of the semi-conductor test equipment by this invention.
[0024] The inspection wafer 11 consists of the doubly-supported beam or a diaphragm 12 (a diaphragm explains henceforth), a probe 13, and a through tube 14. The probe 13 is formed in the diaphragm 12 section, and the dozens of micrometers probe 13 is projected from several micrometers from the base of the inspection wafer 11. Same number individual formation of the through tube 14 is carried out with the probe 13, and the whole surface of the inspection wafer 11 is covered with the silicon oxide film 15. A probe 13 and wiring 16 are formed on the silicon oxide film 15. Wiring 16 is formed even to the secondary electrode pad 17 formed in the opposite side side of the inspection wafer 11 through each through tube 14 from each probe 13.
[0025] Drawing 2 is the sectional view showing one example of the structure of the semi-conductor test equipment by this invention.
[0026] Vacuum adsorption of the **-ed wafer 21 is carried out in the direction of XYZtheta which is not illustrated at the movable wafer fixed stage 22. The wafer fixed stage 22 can carry out alignment of the probe 13 formed in the inspection wafer 11 explained by drawing 1 , and the primary lateral electrode pad 23 formed in the **-ed wafer 21 with high precision, and can be connected.
[0027] In order to connect electrically to the press device support substrate 24 the secondary electrode pad 17 and external terminal which were formed in the inspection wafer 11, the connection terminal and the internal wiring 26 which are called the POGO pin 25 generally [elastic structure] are formed. It is fixed, after the press device support substrate 24 and the inspection wafer 11 carry out alignment of the POGO pin 25 and the secondary electrode pad 23 and connect. Next, it presses against the **-ed wafer 21 which adsorbed the inspection wafer 11 fixed to the press device support substrate 24 on the wafer fixed stage 22.
[0028] By this, the primary lateral electrode pad 23 and a probe 13 contact, a diaphragm 12 deforms, a fixed load is applied between a probe 13 and the primary lateral electrode pad 23, and a uniform electrical-characteristics inspection is attained in all probes. In addition, although the configuration which equips the wafer fixed stage 22 with the migration device of the direction of XYZtheta here explained, a migration device may be added to both the press device support substrate 24, or the wafer fixed stage 22 and the press device support substrate 24.
[0029] Although the external electrode was connected with the secondary electrode pad 17 formed in the inspection wafer 11 using the POGO pin 25 in the above-mentioned explanation, it is good also as structure using the solder bump as substitution of the POGO pin

25.
[0030] Drawing 3 is the sectional view of the structure which added the press device to the semi-conductor test equipment explained by drawing 2 further.
[0031] When thrust sufficient by the POGO pin 25 or just the solder bump for a diaphragm 12 is not added, in order to press other parts to diaphragm 12 pan, elastomers 41 and 42 are formed. However, an elastomer 41 and the elastic structures other than 42 may be prepared. In addition, in drawing 2 and drawing 3 , the silicon oxide film 15 which covers the whole surface of the inspection wafer 11 is omitted.
[0032] Drawing 4 is the sectional view showing the processing process of the inspection wafer of this invention.
[0033] (a) It is better to make the silicon wafer 11 used as a substrate into 600 micrometers in the diameter of 8 inches, and thickness, and to use the thing of the shape of the **-ed wafer 21 and isomorphism. Thereby, reduction of a manufacturing cost and space-saving-ization of test equipment can be attained. For example, when the **-ed wafer 21 is the diameter of 8 inches, the inspection wafer 11 also has the good diameter of 8 inches.
[0034] (b) Form the silicon oxide film 15 with a thickness of 0.7 micrometers in the front face of a silicon wafer 11. Then, the pattern for silicon etching is formed according to a photolithography process. That is, by applying a photoresist to the front face of the silicon oxide film 15, and using and etching [expose, develop and] the photo mask describing a pattern, the silicon oxide film 15 is removed partially and the pattern which has an opening part is formed. Next, a potassium-hydroxide water solution performs anisotropic etching 35 80-degree C%, a silicon wafer 11 is made to eat away from opening of a silicon oxide pattern, and the probe 13 with a height of 50 micrometers is formed.
[0035] Here, although the silicon oxide film 15 was used for the pattern for etching a silicon wafer 11, a silicon nitride film may be used instead. Moreover, although the potassium-hydroxide water solution was used for the etching reagent of a silicon wafer 11, the other anisotropy etching reagent, for example, tetramethylammonium hydroxide, an ethylenediamine pyrocatechol, a hydrazine, etc. may be used.
[0036] (c) Remove a silicon oxide film pattern and form 1 micrometer of silicon oxide film 15 all over a silicon wafer 11 again. The pattern for silicon etching is formed according to a photolithography process like (b), and the diaphragm 12 with 100 micrometers [in thickness] and a die length of 2mm is formed by anisotropic etching.
[0037] (d) Remove a silicon oxide film pattern and form the silicon oxide film 15 all over a silicon wafer 11. The pattern for silicon etching is formed according to a photolithography process, and a through tube 14 is formed with RIE (Reacrive Ion Etching) equipment. The through tube 14 at this time is 100 micrometers in diameter. However, the magnitude of a through tube is good also in magnitude other than this, if several electrode pad minutes can be formed into the magnitude of each semiconductor chip.
[0038] (e) Remove a silicon oxide film pattern and form 0.5 micrometers of silicon oxide film 15 all over a silicon wafer 11. Since this silicon oxide film 15 is what prevents a short circuit inside [of the current which flows the wiring 16 which connects a probe 13 and the secondary electrode pad 17] an inspection wafer, it may be formed by thickness other than this. Moreover, if it does not fuse not above the silicon oxide film but above 150 degrees C, other insulator layers may be formed.
[0039] (f) Use a sputtering system all over a silicon wafer 11 according to a photolithography process after forming a photoresist pattern in the front face of the silicon oxide film 15, form 0.1 micrometers of chromium film first, and form 1 micrometer of nickel film continuously. Then, the chromium film and nickel film on a photoresist and a photoresist are removed using the lift-off method, and wiring 16 and the secondary electrode pad 17 are formed.
[0040] The membrane formation equipment of wiring 16 and the secondary electrode pad 17 may use not only a sputtering system but vacuum evaporationo equipment, and CVD (Chemical Vapor Deposition) equipment. Moreover, the formation approach of wiring 16 and the secondary electrode pad 17 may form an insulator layer not only all over the lift-off method but all over the inspection wafer 11, and may form it in the whole surface by etching at a photolithography process after forming the thin film for wiring further. In addition, the dry etching or whichever using the wet etching which used the etching reagent, or an ion milling system is sufficient as etching at this time. Furthermore, a wiring material may not be fused above 150 degrees C, but may have conductivity, and the ingredient in which thin film formation is possible, for example, gold, copper, platinum, titanium, cobalt, molybdenum, a tungsten, etc. are sufficient as it.
[0041] Drawing 5 is the side elevation and top view showing the configuration of the probe by this invention.
[0042] (a) is the probe 13 formed in the diaphragm 12 in anisotropy wet etching. Anisotropy wet etching is the processing approach using an etch rate changing with differences in the crystal face of silicon in an alkali system etching reagent. For this reason, in the case of the silicon wafer of a field (100), the probe 13 of the shape of a pyramid surrounded in the field (100) and the field (111) is formed.
[0043] (b) shows the probe in the condition that etching advanced further from (a). (100) In ** (100) which a field, a field (100) and (100) a field, and a field (111) intersect mutually, many crystal faces have appeared besides the field and (111) the field. For this reason, it becomes the configuration in which the crystal face where a dirty rate is quicker than the field (100) and field (111) of a field (110), a field (311), etc. appears.
[0044] (c) is the probe which formed mask patterns, such as silicon oxide, in the front face of a diaphragm 12, and the cylindrical point, the silicon wafer was made to incline, performed dry etching with the ion milling system etc. further, and was formed in the shape of a cone, after forming a projection in the shape of a cylinder by dry etching, such as an RIE system. It is better to perform dry etching, making the silicon wafer made to incline rotate and revolve around the sun at this time.
[0045] (d) is the probe formed in the shape of [of the same path as a point] a cylinder by dry etching, such as an RIE system. (e) And (f) is a probe by compound etching with anisotropy wet etching and dry etching. (e) is the combination of (a) and (d) and (f) is the combination of (c) and (d). Thus, although there is especially no limit in the configuration of a probe 13, since the area of the probe 13 which touches a diaphragm 12 by the approach of (c) from (a) as compared with the point area of a probe 13 is large when the height of a probe 13 is decided, the pitch between probes cannot not much be narrowed.
[0046] Although a configuration like (f) is good from (d) when the pitch between probes is narrow, it is inferior to the configuration of (c) from (a) in reinforcement. Therefore, it is better to determine the configuration of a probe 13, taking into consideration the pitch of a primary lateral electrode pad, thrust, a beam or the amount of deflections of a diaphragm, probe height, etc.
[0047] It is good to, form in the probe 13 of (f) from (a) the flat part which is not etched into the part in contact with the primary lateral electrode at a tip at the time of formation of a probe 13 on the other hand. Formation of the configuration where it sharpened without preparing a flat part at the tip of a probe 13 by anisotropy wet etching will extinguish a mask at the moment of sharpening. Although it

is anisotropy wet etching, unless etching solution temperature etc. is managed to a precision, since dispersion by several% of etching arises, within a silicon wafer, the height of the point of a probe 13 will become an ununiformity.
[0048] However, if a flat part is formed at the tip of a probe 13, the height of a probe 13 will become homogeneity. For this reason, when the probe 13 of the inspection wafer 11 is connected with the primary lateral electrode pad 23 of the **-ed wafer 21, the amount of displacement of all the diaphragms 12 of the inspection wafer 11 becomes fixed. Therefore, since the load of all the probes 13 of the inspection wafer 11 becomes fixed, a uniform and highly precise inspection is attained to all the primary lateral electrode pads 23 of the **-ed wafer 21. In addition, the polygon of a square and not only a round shape but others is sufficient as the configuration of the flat part 61 at the tip of a probe 13.
[0049] Drawing 6 is the array of the primary lateral electrode pad formed in a semiconductor chip.
[0050] It can divide roughly into a pad array at that to which the electrode pad 74 was located in a line with (a) (b) Lord in the shape of a straight line like a microcomputer at the periphery of a semiconductor chip 73 with that with which the electrode pad 72 was mainly located in a line in the shape of about 1 straight line along with the center line of a semiconductor chip 71 like DRAM (read-only storage element). (a) And the dimension of the electrode pads 72 and 73 of each [(b)] is hundreds of micrometer angle from dozens of micrometer angle, and the pitch between pads is also dozens of micrometers to hundreds of micrometers.
[0051] Drawing 7 is the top view showing the structure of the beam by this invention, or a diaphragm.
[0052] (a), (b), and (c) are the objects for semiconductor chips located in a line with the core in the shape of a straight line. (a) is the doubly-supported beam structure by this invention. The probe 13 is formed the piece every to each of the doubly-supported beam 12 formed in the inspection wafer 11. Although the pitch between probes is made to counter the pitch between primary lateral electrode pads, a beam width, beam length, and beam thickness consider as this dimension with all probes, and fix the load concerning a probe.
[0053] (b) is the diaphragm structure by this invention. A slit 81 is formed in the direction in which a probe 13 is located in a line, and the load which makes the amount of deflections of a diaphragm 12 homogeneity, and is applied to each probe 13 is fixed. It is effective, when the pitch between pads of a primary lateral electrode is narrow, or when a probe load wants to increase in doubly-supported beam structure and this tooth space.
[0054] (c) is the structure which formed the slit 81 in the four directions. The probe load is effective to decrease although the pitch between pads of a primary lateral electrode cannot form a doubly-supported beam narrowly. (d), (e), and (f) are the objects for semiconductor chips located in a line with the periphery in the shape of a straight line, and (d) is [(f of (e) of (a)) of (b)] the application of (c). Especially (f) forms in a fylfot type the doubly-supported beam 12 which connects the core where the probe 13 has been arranged, and a periphery, and has the structure of increasing the amount of displacement of a probe 13. If it is made structure which lengthens beam length, such as for example, not only a fylfot type but the eddy coil former, the amount of displacement of a probe can be increased further.
[0055] Drawing 8 is the sectional view and top view showing the structure of the doubly-supported beam by this invention.
[0056] By the isotropic etching using the mixed liquor of the dry etching or the fluoric acid-nitric-acid-acetic acid using an RIE system etc., by forming a radius of circle in the root parts 91 and 92 of a doubly-supported beam 12, the rigidity of a doubly-supported beam 12 and endurance can be increased, and the dependability in repeat inspection can be raised. It is an effective means also in not only a doubly-supported beam but a diaphragm, or a cantilever to form a radius of circle.
[0057] Drawing 9 is the top view and sectional view showing the configuration of the through tube by the etching approach. Both (a) (b) and (c) are formed so that a d= 100-micrometer through tube shall be formed in the silicon wafer of a field (X= 2mm, Y= 2mm, and Z= 600 micrometers) (100), and a through tube may not lap with it mutually, and spacing of L= 100 micrometers may be opened and it may stand in a line.
[0058] (a) forms a through tube 102 from one side of a silicon wafer 101 by anisotropy wet etching. The through tube 102 of the shape of a reverse square drill surrounded by four fields (111) 103 which have about 54.7-degree slant face in anisotropy wet etching is formed. At this time, it is set to D1=2 Z/tan54.7 degree+d=949micrometer and P1=D1+L=1049micrometer, and only four through tubes 102 can be formed in the **2mm silicon wafer 101.
[0059] (b) is what formed the through tube 104 from the both sides of a silicon wafer 101 by anisotropy wet etching, and is carrying out the configuration of the shape of a hard drum which connected the reverse square drill-like through tube. this time -- D2=Z/tan54.7"+ -- d= 524 micrometers and P2=D2+L=624micrometer -- becoming -- the **2mm silicon wafer 101 -- nine pieces -- it can form through tube 104.
[0060] Change does not have (a) and (b) in the quantity which can form the dimension of through tubes 102 and 104d in the **2mm silicon wafer 101 in the place made small, and they have a working limit in anisotropy wet etching.
[0061] On the other hand, (c) forms a through tube 105 in a silicon wafer 101 by dry etching, such as an RIE system. A through tube 105 serves as a mask pattern in an almost perpendicular isomorphism-like configuration mostly for dry etching. For this reason, it is set to D3=d=100micrometer and P3=D3+L=200micrometer, and 100 through tubes 105 will be formed in the **2mm silicon wafer 101.
[0062] Moreover, the working limit of an RIE system may be expressed with an aspect ratio (processing depth / processing width of face). Especially the aspect ratio in the case of an ICP-RIE system is called 15 to 20. When processing the silicon wafer 101 with a thickness of 600 micrometers from one side, the minimum processing dimension of a through tube 105 is set to 30 to 40 micrometers. Furthermore, when processing it from both sides, the minimum processing dimension of a through tube 105 is set to 15 to 20 micrometers. Therefore, thousands of pieces can be formed in the **2mm silicon wafer 101. Therefore, right above each semiconductor chip, the through tube of the electrode pad formed in each semiconductor chip and the same number can be formed. Wiring can be shortened by this and wiring resistance can also be reduced.
[0063] Drawing 10 is the perspective view showing the **-ed wafer and the whole inspection wafer outline by this invention. Hundreds of semiconductor chips 111 are formed in the **-ed wafer 21, and 100 and dozens of electrode pads 23 are formed in each semiconductor chip 111 from dozens of pieces. Moreover, the doubly-supported beam or the diaphragm 12 is formed in the inspection wafer 11 the semiconductor chip 111 of the **-ed wafer 21, the same number, or more than it, the electrode pad 23 formed in the semiconductor chip 111 at each doubly-supported beam or diaphragm 12 is countered, and the probe is formed. Furthermore, a through tube 14 is formed around each doubly-supported beam or a diaphragm 12 at the inspection wafer 11, and wiring from each probe is taken out from a through tube 14.
[0064] Drawing 11 is the sectional view showing the structure of the burn-in checking pack by this invention. The doubly-supported beam 12 or diaphragm 12 with easy deformation for the inspection wafer 11 is formed, and the probe 13 is formed in the doubly-

supported beam 12 or the diaphragm 12. An inspection wafer is formed in a **-ed wafer, the same size, or the size not more than it through the processing process explained by drawing 5 . Moreover, it is also possible to cut and combine the inspection wafer of 6 inches of diameters to the **-ed wafer of 8 inches of diameters, and to, carry out package inspection of the **-ed wafer of 8 inches of diameters for example. This is a thing in consideration of the yield etc., for example, even when some inspection wafers are damaged, it is possible to reduce a manufacturing cost by exchanging easily.

[0065] Moreover, by burn-in inspection, in order to perform electric measurement of long duration at the elevated temperature of 150-degree-C order, a location gap of the probe by thermal expansion etc. is not generated by using for the inspection wafer 11 the silicon which is the same quality of the material as the **-ed wafer 21. The **-ed wafer 21 is being fixed to the wafer fixed stage 22 by the vacuum chuck. Moreover, the inspection wafer 11 is fixed to the press device support substrate 24. It can move in the direction of XYZtheta and, thereby, the **-ed wafer 21 and the inspection wafer 11 can carry out alignment of the wafer fixed stage 22 with high precision. The whole is fixed in the burn-in checking pack 121 after alignment. The quality of the material of the burn-in checking pack 121 has small heat deformation above 150 degrees C, and what has a small coefficient-of-thermal-expansion difference with silicon, such as alumimium nitride and Invar, is good.

[0066] However, the terminal 122 for taking out the wiring 26 for electric measurement with the electrode pad 23 formed in the **-ed wafer 21 and the probe 13 formed in the inspection wafer 11 is formed in the burn-in checking pack 121. Generally, although it is necessary to connect the probe formed in all tens of thousands of electrode pads formed in hundreds of chips formed in the **-ed wafer in burn-in inspection at the inspection wafer, electric measurement can be easily performed by using the burn-in checking pack of this invention.

[0067] Drawing 12 is the sectional view showing the outline of the peripheral device of the burn-in checking pack by this invention. A thermostat 132 is in burn-in test equipment 131, and two or more burn-in checking packs 121 are arranged in the thermostat 132. Temperature management of a thermostat 132 is controlled by the temperature controller 133. The wiring 134 of tens of thousands of has led to the burn-in checking pack 121, and it connects with the circuit tester circuit 136 through the high-speed switching circuit 135. The high-speed switching circuit 135 is for changing wiring 134, and can decrease in number the number of input wiring of the circuit tester circuit 136.

[0068] Moreover, since said high-speed switching circuit 135 is a product made from silicon, it makes a high-speed switching circuit to the inspection wafer 11 in the burn-in checking pack 121, and can also make it the structure where wiring from the burn-in checking pack 121 was decreased sharply.

[0069] The technique of this burn-in checking pack can be applied also to probing test equipment. For this reason, it can inspect on wafer level and cost reduction by shortening of inspection time amount can be planned. Moreover, it not only forms only each semiconductor chip 111 and same number which were formed in the **-ed wafer 21 formed in the inspection wafer 11, but more than it is sufficient. Even when it becomes impossible for the probe 13 formed in the inspection wafer 11 to use it by a life etc. by this, **-ed wafer package inspection is again attained only by changing the location of the inspection wafer 11 and the **-ed wafer 21.

[0070] Above this inventions were applied to probing test equipment and burn-in test equipment, and the result of 0.5ohms or less and the test frequency of 200MHz or more in the contact resistance of the wiring 16 of an inspection wafer was obtained. Moreover, the life of the probe 13 at that time was 300,000 times or more. Moreover, since this invention can ensure inspection of the electrode pad of a **-ed wafer, it can be used for the electrode for LSI and the object for detailed pattern drawers, or the connector for connection. Furthermore, since silicon is used for the probe formation substrate in this invention, it is possible to incorporate or form resistance or a circuit at the time of said probe formation substrate processing.

[0071]

[Effect of the Invention] According to this invention, in the electrical-characteristics inspection process which is one process of a semiconductor device production process, large field package inspection of the electrode pad of analyte is attained.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the inspection approach of of the semiconductor device or semiconductor device formed on the wafer, especially relates to the test equipment for electrical-characteristics measurement in semi-conductor production processes, such as probing inspection and burn-in inspection.

[Translation done.]

PRIOR ART

[Description of the Prior Art] It is divided roughly into a last process until it forms a circuit in a silicon wafer front face, and a back process until it separates this silicon wafer for the chip according to individual and closes with resin, a ceramic, etc. in semiconductor devices, such as IC (integrated circuit) and LSI (large-scale integrated circuit). In these semiconductor devices, electrical-characteristics inspection of each circuit is conducted in the predetermined phase in a last process, and the judgment of an excellent article and a defective is performed per chip. It can classify to that the above-mentioned electrical-characteristics inspection is thermal in probing inspection which distinguishes the quality of the flow between each circuit, and an about 150-degree C elevated temperature, and burn-in inspection which carries out acceleration sorting of the defect by giving electrical stress to a circuit.
[0003] probing inspection and burn-in inspection -- the fundamental connecting means of a **-ed wafer and external check system -- abbreviation -- it is the same. That is, the approach of pressing a conductive detailed probe mechanically separately to the electrode pad of each aluminium alloy with an angle [dozens thru/or hundreds of micrometer angle] by which patterning was carried out, and a thickness of about 1 micrometer, or other alloys in dozens thru/or hundreds of micrometer pitch is adopted on the **-ed wafer.
[0004] Conventionally, the structure of the used probe is shown in drawing 13 and drawing 14 .
[0005] Each probe 141 is mainly the thin needle of 10 micrometers of tip parameters, and 10mm of die-length numbers in the product made from a tungsten, and it is fixed or fabricated in drawing 13 by the substrate 142 and the insulating fixture 143 so that a tip location may correspond to each electrode pad of a **-ed wafer.
[0006] the probe 151 of each [drawing 14] -- mainly -- plating -- accumulating -- it is the metal projection of the shape of a pyramid which formed the metal projection of the shape of a fabricated semi-sphere, or the anisotropic etching hole of a silicon substrate as a plating mold etc., and this aggregate is formed in the front face of the organic thin films 152, such as polyimide.
[0007] Moreover, JP,6-123746,A, JP,7-7052,A and JP,8-50146,A, and JP,9-243663,A are exhibited as a means to solve the trouble of the two above-mentioned examples mentioned later.
[0008] In JP,6-123746,A, slitting was put into the card in which elastic deformation is possible, two or more probe needles in which elastic deformation is possible were formed in homogeneity, and two or more contact which can contact the electrode of a semiconductor device is prepared according to the individual at each point of two or more of these probe needles.
[0009] moreover -- JP,7-7052,A -- single crystal silicon, silicon oxide, silicon nitride, polish recon, or a metal layer -- at least -- much more -- since -- it considers as the becoming cantilever structure, and this cantilever structure is further held by the insulating substrate in which the metallic film for a flow was formed on that front face and in which the flow circuit pattern was formed, and it is considering as the probe for electrical property measurement.
[0010] On the other hand, in JP,9-243663,A, a silicon substrate is processed in the shape of a diaphragm, and the probe for filling up with an elastomer the diaphragm section of the structure in which two or more contact probes were formed to the contact side, and measuring an electrical property is formed.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, in the electrical-characteristics inspection process which is one process of a semiconductor device production process, large field package inspection of the electrode pad of analyte is attained.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] There was a trouble as shown below by the inspection approach of a semiconductor device which was stated with the above and the conventional technique.
[0012] It was difficult to need great time amount for positioning and fixing each probe with high precision with the probe structure shown in drawing 13 , and to mass-produce the probe structure cheaply. Moreover, since many fields for positioning and fixing each probe were needed, it is difficult to arrange many probes by the inside of a substrate, and the number of electrode pads or the number of chips which can be inspected at once was restricted. Furthermore, since each probe length was as large as about dozens of mm, the regulation capacity in each probe was large, and parenchyma was impossible for inspection of a high-speed device about 100MHz or more.
[0013] Moreover, in order to destroy the insulating natural oxidation film with which the radius of curvature of each end of the probe was large with the film, and was formed in the electrode pad front face of a **-ed wafer Since the actuation which carries out the scribe (marking-off) of a big press load and the electrode pad front face is needed, Wear of the end of the probe was brought forward, and there was a problem with which the dust of the electrode pad generated by about [that the life (count of durable inspection) of a probe was short] and the scribe pollutes the environment in semiconductor device manufacture.
[0014] Moreover, since a probe was arranged in a detailed pitch on organic thin film front faces, such as polyimide, in the probe structure shown in drawing 14 corresponding to the electrode pad of a **-ed wafer, it was difficult to absorb independently dispersion in the distance of the probe produced by the curvature of a **-ed wafer, or dispersion of the height of a probe, and a corresponding electrode pad. Moreover, since organic thin films, such as polyimide with which coefficient of linear expansion differs from a **-ed wafer greatly, were used as the base material, by burn-in inspection conducted in an about 150-degree C elevated temperature, the big differential thermal expansion arose between **-ed wafers, and there was a case where the location gap with an electrode pad and a probe arose, with the probe in the location distant from the core.
[0015] Moreover, in JP,6-123746,A, since a card consisted of synthetic resin or a metal, formation of two or more probe needles in which elastic deformation is possible was difficult for probe arrangement in the detailed pitch corresponding to the electrode pad location of a **-ed wafer, i.e., each.
[0016] In JP,7-7052,A, in order to join anew each cantilever probe formed with the silicon system base material to an insulating-substrate front face different from it, the manufacture yield fell, and there was a problem of an ununiformity in the height of the probe of further each.
[0017] Although it is indicated by JP,9-243663,A that the diaphragm section formed in the silicon substrate along with distortion of a **-ed wafer deforms using an elastomer (elastic material), by this method, dispersion in the thickness of a diaphragm is not taken into consideration, and when a diaphragm with dispersion in a wave or thickness is made to deform, control of the height of a contact probe cannot be performed. Therefore, since the depth direction of the pad for electrical-characteristics measurement of a **-ed wafer is uncontrollable, when thrust is insufficient, the part which does not contact the pad section for electrical-characteristics measurement of a **-ed wafer comes out. Moreover, when thrust was put too much, it sank into the pad section for electrical-characteristics measurement of a **-ed wafer deeply, and there was a problem which destroys a **-ed wafer.
[0018] Moreover, since wiring for the electrical installation of the tip of a probe and external check system is formed in the same front face as the probe forming face in a substrate for which the above-mentioned probe structure, It does not obtain. all external connection terminals -- the near periphery of a base material -- concentrating -- not forming -- It was difficult to limit the field of this external connection terminal which can be formed, and to connect many probes with the exterior electrically, for example, large field coincidence inspection of inspecting all the electrode pads of a **-ed wafer collectively was difficult.
[0019] The purpose of this invention solves many troubles described until now, enables large field coincidence inspection which says that all the electrode pads of a **-ed wafer carry out package inspection in electrical-characteristics inspection of a semiconductor device, raises the manufacture yield by it, reduces a manufacturing cost, is cheap and is to obtain the semiconductor device which has high-reliability.

[Translation done.]

MEANS

[Means for Solving the Problem] It can attain by establishing the device which presses the probe or the probe periphery of the device which presses or fixes the **-ed wafer with which a semiconductor device and test equipment were contacted directly, the beam structure or the diaphragm structure where of a probe could change with thrust to the substrate with which the probe was formed in the approach of inspecting a semiconductor device was formed, connecting electrically, and the electrode pad of a checking semiconductor device was formed in order to attain the above-mentioned purpose, or said substrate. Moreover, it is good to use silicon for the substrate with which the above-mentioned probe was formed, to constitute a probe from silicon, metals, or those composites, and to use the structure currently wired at the rear-face side of a probe formation substrate with wiring using a conductive ingredient through an insulating material. Moreover, it is possible by having the flat-surface section in the point of this probe to form probe height in homogeneity with high precision moreover.
[0021] The structure which the structure of the probe formed in the doubly-supported beam which became independent separately was desirable, formed the probe in the longitudinal plane of symmetry, and formed the beam in the fylfot type configuration for the perimeter may be used. Anisotropic etching or dry etching is used for processing of the structure including these beams. By using ICP-RIE (InductivelyCoupled Plasma-Reactive Ion Etching) equipment for the above-mentioned dry etching, it is possible to form spacing of a beam and a beam narrowly, and it can respond also to ** pitch-ization of a device.
[0022] Wiring uses anisotropic etching or dry etching for an inspection wafer, makes this substrate penetrate and uses the approach of wiring electrically the probe forming face and rear face of this substrate using a spatter, vacuum evaporationo, or plating. Moreover, the through tube of an inspection wafer has the good method formed using dry etching. Furthermore, the semiconductor device or electronic parts inspected using above-mentioned structure and an above-mentioned approach is very cheap, and can be offered.
[0023]
[Embodiment of the Invention] Hereafter, the example of this invention is explained using a drawing. Drawing 1 is the sectional view showing the 1 actual example of the structure of the inspection wafer of the semi-conductor test equipment by this invention.
[0024] The inspection wafer 11 consists of the doubly-supported beam or a diaphragm 12 (a diaphragm explains henceforth), a probe 13, and a through tube 14. The probe 13 is formed in the diaphragm 12 section, and the dozens of micrometers probe 13 is projected from several micrometers from the base of the inspection wafer 11. Same number individual formation of the through tube 14 is carried out with the probe 13, and the whole surface of the inspection wafer 11 is covered with the silicon oxide film 15. A probe 13 and wiring 16 are formed on the silicon oxide film 15. Wiring 16 is formed even to the secondary electrode pad 17 formed in the opposite side side of the inspection wafer 11 through each through tube 14 from each probe 13.
[0025] Drawing 2 is the sectional view showing one example of the structure of the semi-conductor test equipment by this invention.
[0026] Vacuum adsorption of the **-ed wafer 21 is carried out in the direction of XYZtheta which is not illustrated at the movable wafer fixed stage 22. The wafer fixed stage 22 can carry out alignment of the probe 13 formed in the inspection wafer 11 explained by drawing 1 , and the primary lateral electrode pad 23 formed in the **-ed wafer 21 with high precision, and can be connected.
[0027] In order to connect electrically to the press device support substrate 24 the secondary electrode pad 17 and external terminal which were formed in the inspection wafer 11, the connection terminal and the internal wiring 26 which are called the POGO pin 25 generally [elastic structure] are formed. It is fixed, after the press device support substrate 24 and the inspection wafer 11 carry out alignment of the POGO pin 25 and the secondary electrode pad 23 and connect. Next, it presses against the **-ed wafer 21 which adsorbed the inspection wafer 11 fixed to the press device support substrate 24 on the wafer fixed stage 22.
[0028] By this, the primary lateral electrode pad 23 and a probe 13 contact, a diaphragm 12 deforms, a fixed load is applied between a probe 13 and the primary lateral electrode pad 23, and a uniform electrical-characteristics inspection is attained in all probes. In addition, although the configuration which equips the wafer fixed stage 22 with the migration device of the direction of XYZtheta here explained, a migration device may be added to both the press device support substrate 24, or the wafer fixed stage 22 and the press device support substrate 24.
[0029] Although the external electrode was connected with the secondary electrode pad 17 formed in the inspection wafer 11 using the POGO pin 25 in the above-mentioned explanation, it is good also as structure using the solder bump as substitution of the POGO pin 25.
[0030] Drawing 3 is the sectional view of the structure which added the press device to the semi-conductor test equipment explained by drawing 2 further.
[0031] When thrust sufficient by the POGO pin 25 or just the solder bump for a diaphragm 12 is not added, in order to press other parts to diaphragm 12 pan, elastomers 41 and 42 are formed. However, an elastomer 41 and the elastic structures other than 42 may be prepared. In addition, in drawing 2 and drawing 3 , the silicon oxide film 15 which covers the whole surface of the inspection wafer 11 is omitted.
[0032] Drawing 4 is the sectional view showing the processing process of the inspection wafer of this invention.
[0033] (a) It is better to make the silicon wafer 11 used as a substrate into 600 micrometers in the diameter of 8 inches, and thickness, and to use the thing of the shape of the **-ed wafer 21 and isomorphism. Thereby, reduction of a manufacturing cost and space-saving-ization of test equipment can be attained. For example, when the **-ed wafer 21 is the diameter of 8 inches, the inspection wafer 11 also has the good diameter of 8 inches.

[0034] (b) Form the silicon oxide film 15 with a thickness of 0.7 micrometers in the front face of a silicon wafer 11. Then, the pattern for silicon etching is formed according to a photolithography process. That is, by applying a photoresist to the front face of the silicon oxide film 15, and using and etching [expose, develop and] the photo mask describing a pattern, the silicon oxide film 15 is removed partially and the pattern which has an opening part is formed. Next, a potassium-hydroxide water solution performs anisotropic etching 35 80-degree C%, a silicon wafer 11 is made to eat away from opening of a silicon oxide pattern, and the probe 13 with a height of 50 micrometers is formed.
[0035] Here, although the silicon oxide film 15 was used for the pattern for etching a silicon wafer 11, a silicon nitride film may be used instead. Moreover, although the potassium-hydroxide water solution was used for the etching reagent of a silicon wafer 11, the other anisotropy etching reagent, for example, tetramethylammonium hydroxide, an ethylenediamine pyrocatechol, a hydrazine, etc. may be used.
[0036] (c) Remove a silicon oxide film pattern and form 1 micrometer of silicon oxide film 15 all over a silicon wafer 11 again. The pattern for silicon etching is formed according to a photolithography process like (b), and the diaphragm 12 with 100 micrometers [in thickness] and a die length of 2mm is formed by anisotropic etching.
[0037] (d) Remove a silicon oxide film pattern and form the silicon oxide film 15 all over a silicon wafer 11. The pattern for silicon etching is formed according to a photolithography process, and a through tube 14 is formed with RIE (Reacrive Ion Etching) equipment. The through tube 14 at this time is 100 micrometers in diameter. However, the magnitude of a through tube is good also in magnitude other than this, if several electrode pad minutes can be formed into the magnitude of each semiconductor chip.
[0038] (e) Remove a silicon oxide film pattern and form 0.5 micrometers of silicon oxide film 15 all over a silicon wafer 11. Since this silicon oxide film 15 is what prevents a short circuit inside [of the current which flows the wiring 16 which connects a probe 13 and the secondary electrode pad 17] an inspection wafer, it may be formed by thickness other than this. Moreover, if it does not fuse not above the silicon oxide film but above 150 degrees C, other insulator layers may be formed.
[0039] (f) Use a sputtering system all over a silicon wafer 11 according to a photolithography process after forming a photoresist pattern in the front face of the silicon oxide film 15, form 0.1 micrometers of chromium film first, and form 1 micrometer of nickel film continuously. Then, the chromium film and nickel film on a photoresist and a photoresist are removed using the lift-off method, and wiring 16 and the secondary electrode pad 17 are formed.
[0040] The membrane formation equipment of wiring 16 and the secondary electrode pad 17 may use not only a sputtering system but vacuum evaporationo equipment, and CVD (Chemical Vapor Deposition) equipment. Moreover, the formation approach of wiring 16 and the secondary electrode pad 17 may form an insulator layer not only all over the lift-off method but all over the inspection wafer 11, and may form it in the whole surface by etching at a photolithography process after forming the thin film for wiring further. In addition, the dry etching or whichever using the wet etching which used the etching reagent, or an ion milling system is sufficient as etching at this time. Furthermore, a wiring material may not be fused above 150 degrees C, but may have conductivity, and the ingredient in which thin film formation is possible, for example, gold, copper, platinum, titanium, cobalt, molybdenum, a tungsten, etc. are sufficient as it.
[0041] Drawing 5 is the side elevation and top view showing the configuration of the probe by this invention.
[0042] (a) is the probe 13 formed in the diaphragm 12 in anisotropy wet etching. Anisotropy wet etching is the processing approach using an etch rate changing with differences in the crystal face of silicon in an alkali system etching reagent. For this reason, in the case of the silicon wafer of a field (100), the probe 13 of the shape of a pyramid surrounded in the field (100) and the field (111) is formed.
[0043] (b) shows the probe in the condition that etching advanced further from (a). (100) In ** (100) which a field, a field (100) and (100) a field, and a field (111) intersect mutually, many crystal faces have appeared besides the field and (111) the field. For this reason, it becomes the configuration in which the crystal face where a dirty rate is quicker than the field (100) and field (111) of a field (110), a field (311), etc. appears.
[0044] (c) is the probe which formed mask patterns, such as silicon oxide, in the front face of a diaphragm 12, and the cylindrical point, the silicon wafer was made to incline, performed dry etching with the ion milling system etc. further, and was formed in the shape of a cone, after forming a projection in the shape of a cylinder by dry etching, such as an RIE system. It is better to perform dry etching, making the silicon wafer made to incline rotate and revolve around the sun at this time.
[0045] (d) is the probe formed in the shape of [of the same path as a point] a cylinder by dry etching, such as an RIE system. (e) And (f) is a probe by compound etching with anisotropy wet etching and dry etching. (e) is the combination of (a) and (d) and (f) is the combination of (c) and (d). Thus, although there is especially no limit in the configuration of a probe 13, since the area of the probe 13 which touches a diaphragm 12 by the approach of (c) from (a) as compared with the point area of a probe 13 is large when the height of a probe 13 is decided, the pitch between probes cannot not much be narrowed.
[0046] Although a configuration like (f) is good from (d) when the pitch between probes is narrow, it is inferior to the configuration of (c) from (a) in reinforcement. Therefore, it is better to determine the configuration of a probe 13, taking into consideration the pitch of a primary lateral electrode pad, thrust, a beam or the amount of deflections of a diaphragm, probe height, etc.
[0047] It is good to, form in the probe 13 of (f) from (a) the flat part which is not etched into the part in contact with the primary lateral electrode at a tip at the time of formation of a probe 13 on the other hand. Formation of the configuration where it sharpened without preparing a flat part at the tip of a probe 13 by anisotropy wet etching will extinguish a mask at the moment of sharpening. Although it is anisotropy wet etching, unless etching solution temperature etc. is managed to a precision, since dispersion by several% of etching arises, within a silicon wafer, the height of the point of a probe 13 will become an ununiformity.
[0048] However, if a flat part is formed at the tip of a probe 13, the height of a probe 13 will become homogeneity. For this reason, when the probe 13 of the inspection wafer 11 is connected with the primary lateral electrode pad 23 of the **-ed wafer 21, the amount of displacement of all the diaphragms 12 of the inspection wafer 11 becomes fixed. Therefore, since the load of all the probes 13 of the inspection wafer 11 becomes fixed, a uniform and highly precise inspection is attained to all the primary lateral electrode pads 23 of the **-ed wafer 21. In addition, the polygon of a square and not only a round shape but others is sufficient as the configuration of the flat part 61 at the tip of a probe 13.
[0049] Drawing 6 is the array of the primary lateral electrode pad formed in a semiconductor chip.
[0050] It can divide roughly into a pad array at that to which the electrode pad 74 was located in a line with (a) (b) Lord in the shape of a straight line like a microcomputer at the periphery of a semiconductor chip 73 with that with which the electrode pad 72 was mainly located in a line in the shape of about 1 straight line along with the center line of a semiconductor chip 71 like DRAM (read-only

storage element). (a) And the dimension of the electrode pads 72 and 73 of each [(b)] is hundreds of micrometer angle from dozens of micrometer angle, and the pitch between pads is also dozens of micrometers to hundreds of micrometers.
[0051] Drawing 7 is the top view showing the structure of the beam by this invention, or a diaphragm.
[0052] (a), (b), and (c) are the objects for semiconductor chips located in a line with the core in the shape of a straight line. (a) is the doubly-supported beam structure by this invention. The probe 13 is formed the piece every to each of the doubly-supported beam 12 formed in the inspection wafer 11. Although the pitch between probes is made to counter the pitch between primary lateral electrode pads, a beam width, beam length, and beam thickness consider as this dimension with all probes, and fix the load concerning a probe.
[0053] (b) is the diaphragm structure by this invention. A slit 81 is formed in the direction in which a probe 13 is located in a line, and the load which makes the amount of deflections of a diaphragm 12 homogeneity, and is applied to each probe 13 is fixed. It is effective, when the pitch between pads of a primary lateral electrode is narrow, or when a probe load wants to increase in doubly-supported beam structure and this tooth space.
[0054] (c) is the structure which formed the slit 81 in the four directions. The probe load is effective to decrease although the pitch between pads of a primary lateral electrode cannot form a doubly-supported beam narrowly. (d), (e), and (f) are the objects for semiconductor chips located in a line with the periphery in the shape of a straight line, and (d) is [(f of (e) of (a)) of (b)] the application of (c). Especially (f) forms in a fylfot type the doubly-supported beam 12 which connects the core where the probe 13 has been arranged, and a periphery, and has the structure of increasing the amount of displacement of a probe 13. If it is made structure which lengthens beam length, such as for example, not only a fylfot type but the eddy coil former, the amount of displacement of a probe can be increased further.
[0055] Drawing 8 is the sectional view and top view showing the structure of the doubly-supported beam by this invention.
[0056] By the isotropic etching using the mixed liquor of the dry etching or the fluoric acid-nitric-acid-acetic acid using an RIE system etc., by forming a radius of circle in the root parts 91 and 92 of a doubly-supported beam 12, the rigidity of a doubly-supported beam 12 and endurance can be increased, and the dependability in repeat inspection can be raised. It is an effective means also in not only a doubly-supported beam but a diaphragm, or a cantilever to form a radius of circle.
[0057] Drawing 9 is the top view and sectional view showing the configuration of the through tube by the etching approach. Both (a) (b) and (c) are formed so that a d= 100-micrometer through tube shall be formed in the silicon wafer of a field (X= 2mm, Y= 2mm, and Z= 600 micrometers) (100), and a through tube may not lap with it mutually, and spacing of L= 100 micrometers may be opened and it may stand in a line.
[0058] (a) forms a through tube 102 from one side of a silicon wafer 101 by anisotropy wet etching. The through tube 102 of the shape of a reverse square drill surrounded by four fields (111) 103 which have about 54.7-degree slant face in anisotropy wet etching is formed. At this time, it is set to D1=2 Z/tan54.7 degree+d=949micrometer and P1=D1+L=1049micrometer, and only four through tubes 102 can be formed in the **2mm silicon wafer 101.
[0059] (b) is what formed the through tube 104 from the both sides of a silicon wafer 101 by anisotropy wet etching, and is carrying out the configuration of the shape of a hard drum which connected the reverse square drill-like through tube. this time -- D2=Z/tan54.7"+ -- d= 524 micrometers and P2=D2+L=624micrometer -- becoming -- the **2mm silicon wafer 101 -- nine pieces -- it can form through tube 104.
[0060] Change does not have (a) and (b) in the quantity which can form the dimension of through tubes 102 and 104d in the **2mm silicon wafer 101 in the place made small, and they have a working limit in anisotropy wet etching.
[0061] On the other hand, (c) forms a through tube 105 in a silicon wafer 101 by dry etching, such as an RIE system. A through tube 105 serves as a mask pattern in an almost perpendicular isomorphism-like configuration mostly for dry etching. For this reason, it is set to D3=d=100micrometer and P3=D3+L=200micrometer, and 100 through tubes 105 will be formed in the **2mm silicon wafer 101.
[0062] Moreover, the working limit of an RIE system may be expressed with an aspect ratio (processing depth / processing width of face). Especially the aspect ratio in the case of an ICP-RIE system is called 15 to 20. When processing the silicon wafer 101 with a thickness of 600 micrometers from one side, the minimum processing dimension of a through tube 105 is set to 30 to 40 micrometers. Furthermore, when processing it from both sides, the minimum processing dimension of a through tube 105 is set to 15 to 20 micrometers. Therefore, thousands of pieces can be formed in the **2mm silicon wafer 101. Therefore, right above each semiconductor chip, the through tube of the electrode pad formed in each semiconductor chip and the same number can be formed. Wiring can be shortened by this and wiring resistance can also be reduced.
[0063] Drawing 10 is the perspective view showing the **-ed wafer and the whole inspection wafer outline by this invention. Hundreds of semiconductor chips 111 are formed in the **-ed wafer 21, and 100 and dozens of electrode pads 23 are formed in each semiconductor chip 111 from dozens of pieces. Moreover, the doubly-supported beam or the diaphragm 12 is formed in the inspection wafer 11 the semiconductor chip 111 of the **-ed wafer 21, the same number, or more than it, the electrode pad 23 formed in the semiconductor chip 111 at each doubly-supported beam or diaphragm 12 is countered, and the probe is formed. Furthermore, a through tube 14 is formed around each doubly-supported beam or a diaphragm 12 at the inspection wafer 11, and wiring from each probe is taken out from a through tube 14.
[0064] Drawing 11 is the sectional view showing the structure of the burn-in checking pack by this invention. The doubly-supported beam 12 or diaphragm 12 with easy deformation for the inspection wafer 11 is formed, and the probe 13 is formed in the doubly-supported beam 12 or the diaphragm 12. An inspection wafer is formed in a **-ed wafer, the same size, or the size not more than it through the processing process explained by drawing 5 . Moreover, it is also possible to cut and combine the inspection wafer of 6 inches of diameters to the **-ed wafer of 8 inches of diameters, and to, carry out package inspection of the **-ed wafer of 8 inches of diameters for example. This is a thing in consideration of the yield etc., for example, even when some inspection wafers are damaged, it is possible to reduce a manufacturing cost by exchanging easily.
[0065] Moreover, by burn-in inspection, in order to perform electric measurement of long duration at the elevated temperature of 150-degree-C order, a location gap of the probe by thermal expansion etc. is not generated by using for the inspection wafer 11 the silicon which is the same quality of the material as the **-ed wafer 21. The **-ed wafer 21 is being fixed to the wafer fixed stage 22 by the vacuum chuck. Moreover, the inspection wafer 11 is fixed to the press device support substrate 24. It can move in the direction of XYZtheta and, thereby, the **-ed wafer 21 and the inspection wafer 11 can carry out alignment of the wafer fixed stage 22 with high precision. The whole is fixed in the burn-in checking pack 121 after alignment. The quality of the material of the burn-in checking pack 121 has small heat deformation above 150 degrees C, and what has a small coefficient-of-thermal-expansion difference with silicon,

such as alumimium nitride and Invar, is good.
[0066] However, the terminal 122 for taking out the wiring 26 for electric measurement with the electrode pad 23 formed in the **-ed wafer 21 and the probe 13 formed in the inspection wafer 11 is formed in the burn-in checking pack 121. Generally, although it is necessary to connect the probe formed in all tens of thousands of electrode pads formed in hundreds of chips formed in the **-ed wafer in burn-in inspection at the inspection wafer, electric measurement can be easily performed by using the burn-in checking pack of this invention.
[0067] Drawing 12 is the sectional view showing the outline of the peripheral device of the burn-in checking pack by this invention. A thermostat 132 is in burn-in test equipment 131, and two or more burn-in checking packs 121 are arranged in the thermostat 132. Temperature management of a thermostat 132 is controlled by the temperature controller 133. The wiring 134 of tens of thousands of has led to the burn-in checking pack 121, and it connects with the circuit tester circuit 136 through the high-speed switching circuit 135. The high-speed switching circuit 135 is for changing wiring 134, and can decrease in number the number of input wiring of the circuit tester circuit 136.
[0068] Moreover, since said high-speed switching circuit 135 is a product made from silicon, it makes a high-speed switching circuit to the inspection wafer 11 in the burn-in checking pack 121, and can also make it the structure where wiring from the burn-in checking pack 121 was decreased sharply.
[0069] The technique of this burn-in checking pack can be applied also to probing test equipment. For this reason, it can inspect on wafer level and cost reduction by shortening of inspection time amount can be planned. Moreover, it not only forms only each semiconductor chip 111 and same number which were formed in the **-ed wafer 21 formed in the inspection wafer 11, but more than it is sufficient. Even when it becomes impossible for the probe 13 formed in the inspection wafer 11 to use it by a life etc. by this, **-ed wafer package inspection is again attained only by changing the location of the inspection wafer 11 and the **-ed wafer 21.
[0070] Above this inventions were applied to probing test equipment and burn-in test equipment, and the result of 0.5ohms or less and the test frequency of 200MHz or more in the contact resistance of the wiring 16 of an inspection wafer was obtained. Moreover, the life of the probe 13 at that time was 300,000 times or more. Moreover, since this invention can ensure inspection of the electrode pad of a **-ed wafer, it can be used for the electrode for LSI and the object for detailed pattern drawers, or the connector for connection. Furthermore, since silicon is used for the probe formation substrate in this invention, it is possible to incorporate or form resistance or a circuit at the time of said probe formation substrate processing.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the inspection wafer about one example of this invention.
[Drawing 2] It is the sectional view of the inspection object structure about one example of this invention.
[Drawing 3] It is the sectional view of the inspection object structure about other one example of this invention.
[Drawing 4] It is the sectional view of the inspection wafer processing process about one example of this invention.
[Drawing 5] It is the side elevation and top view of a probe about one example of this invention.
[Drawing 6] It is the top view showing the array of the electrode pad of a semiconductor chip.
[Drawing 7] It is the top view showing the beam and diaphragm about one example of this invention.
[Drawing 8] It is the sectional view and top view about one example of this invention.
[Drawing 9] It is the top view and sectional view about one example of this invention.
[Drawing 10] It is a perspective view about one example of this invention.
[Drawing 11] It is a sectional view about one example of this invention.
[Drawing 12] It is a sectional view about one example of this invention.
[Drawing 13] It is a sectional view about the conventional technique.
[Drawing 14] It is a sectional view about other conventional techniques.
[** of a sign]
11 -- An inspection wafer, 12 -- A doubly-supported beam or a diaphragm, 13 -- Probe, 14 [-- Secondary electrode pad,] -- A through tube, 15 -- An insulator layer, 16 -- Wiring, 17 21 -- A **-ed wafer, 22 -- A wafer fixed stage, 23 -- Primary lateral electrode pad, 24 [-- Solder ball,] -- A press device support substrate, 25 -- A POGO pin, 26 -- Internal wiring, 31 41 42 [-- Electrode pad,] -- An elastomer, 61 -- A flat part, 71 -- A semiconductor chip, 72 73 [-- Radius of circle,] -- A semiconductor chip, 74 -- An electrode pad, 81 -- 91 A slit, 92 101 -- A silicon wafer, 102 -- A through tube, 103 -- (111) Field, 105 -- A through tube, 111 -- A semiconductor device, 121 -- Burn-in checking pack, 122 [-- Temperature controller,] -- A terminal, 131 -- Burn-in test equipment, 132 -- A thermostat, 133 134 [-- The form width of a silicon wafer, Y / -- The vertical dimension of a silicon wafer, Z / -- The height dimension of a silicon wafer, P1, P2, P3 / -- The pitch between through tubes, d, D1, D2, D3 / -- Through tube aperture width, L / -- Through tube spacing.] -- Wiring, 135 -- A high-speed switching circuit, 136 -- A circuit tester circuit, X

[Translation done.]

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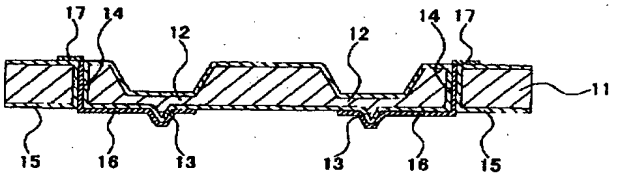
(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地
(72)発明者　細金　敦
茨城県土浦市神立町502番地　株式会社日立製作所機械研究所内
(72)発明者　金丸　昌敏
茨城県土浦市神立町502番地　株式会社日立製作所機械研究所内
(74)代理人　100068504
弁理士　小川　勝男

最終頁に続く

(54)【発明の名称】　半導体検査装置の製造方法

(57)【要約】
【課題】従来の半導体検査装置のプローブでは、プローブの精度上の問題等から複数のプローブで一括して複数の半導体装置を検査することが困難であった。
【解決手段】シリコン基板の表面に被膜を形成し、フォトリソグラフィ（ＦＲ）によるパターニング後にエッチングにより角錐状あるいは円錐状の複数のプローブを形成する工程と、被膜を除去後、再びシリコン基板の表面に被膜を形成し、ＦＲによるパターニング後にエッチングにより梁あるいはダイアフラムを前記プローブ毎に形成する工程と、被膜を除去後、再びシリコン基板の表面に被膜を形成し、ＦＲによるパターニング後にエッチングにより貫通孔を形成する工程と、被膜を除去後、再びシリコン基板の表面に絶縁被膜を形成し、前記絶縁皮膜の表面に金属被膜を形成し、ＦＲによるパターニング後にエッチングにより配線を形成する工程を備えた半導体検査装置の製造方法。

図１



【特許請求の範囲】

【請求項１】シリコン基板の一方側の面に形成された複数のプローブと、前記シリコン基板の他方側の面に形成された複数の電極と、前記複数のプローブと前記複数の電極とを電気的に導通する配線を備えた半導体検査装置の製造方法において、

シリコン基板の表面に被膜を形成し、フォトリソグラフィによるパターニング後にエッチングにより角錐状あるいは円錐状の複数のプローブを形成する工程と、

被膜を除去後、再びシリコン基板の表面に被膜を形成し、フォトリソグラフィによるパターニング後にエッチングにより梁あるいはダイアフラムを前記プローブ毎に形成する工程と、

被膜を除去後、再びシリコン基板の表面に被膜を形成し、フォトリソグラフィによるパターニング後にエッチングにより前記プローブに対応して貫通孔を形成する工程と、

被膜を除去後、再びシリコン基板の表面に絶縁被膜を形成し、前記絶縁皮膜の表面に金属被膜を形成し、フォトリソグラフィによるパターニング後にエッチングにより配線を形成する工程を行うことを特徴とする半導体検査装置の製造方法。

【請求項２】請求項１において、プローブの先端に平坦部を有することを特徴とする半導体検査装置の製造方法。

【請求項３】請求項１において、梁の構造が両持ち梁であることを特徴とする半導体検査装置の製造方法。

【請求項４】シリコン基板の一主面に形成されたプローブと、前記シリコン基板の一主面とは反対の面に形成された電極と、前記プローブと前記電極とを電気的に導通する手段を備えた検査ウエハを用いて、前記プローブを検査対象ウエハの所定の位置に押圧基板により押圧し、前記検査対象ウエハの電気的導通検査を行う半導体検査装置において、

押圧基板による検査ウエハとの接続および押圧を被検ウエハの電極数と同数あるいはそれ以上のポゴピンを用いて行うことを特徴とする半導体検査装置。

【請求項５】請求項４において、押圧基板による検査ウエハとの接続および押圧を被検ウエハの電極数と同数あるいはそれ以上のはんだボールを用いて行うことを特徴とする半導体検査装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はウエハ上に形成された半導体素子あるいは半導体デバイスの検査方法に係り、特にプロービング検査およびバーンイン検査など半導体製造工程における電気的特性測定用の検査装置に関する。

【０００２】

【従来の技術】ＩＣ（集積回路）やＬＳＩ（大規模集積回路）などの半導体素子では、シリコンウエハ表面に回路を形成するまでの前工程と、このシリコンウエハを個別のチップに切り離して樹脂やセラミック等で封止するまでの後工程とに大別される。これらの半導体装置では、前工程中の所定の段階において各回路の電気的特性検査が行われ、チップ単位で良品、不良品の判定が行われる。上記の電気的特性検査は各回路間の導通の良否を判別するプロービング検査と、１５０℃程度の高温中で熱的、電気的ストレスを回路に付与して不良を加速選別するバーンイン検査とに分別できる。

【０００３】プロービング検査、バーンイン検査共、被検ウエハと外部の検査システムとの基本的な接続手段は略同じである。すなわち、被検ウエハ上に数十ないし数百μｍピッチでパターニングされた、数十ないし数百μｍ角、厚さ１μｍ程度の個々のアルミニウム合金あるいはその他の合金の電極パッドに対して、個々に導電性の微細なプローブを機械的に押圧する方法が採用されている。

【０００４】従来、用いられていたプローブの構造を図１３および図１４に示す。

【０００５】図１３では個々のプローブ１４１は主にタングステン製で先端径数十μｍ、長さ数十ｍｍの細針であり、先端位置が被検ウエハの各電極パッドに対応するよう基板１４２および絶縁治具１４３に固定あるいは成形されている。

【０００６】図１４では個々のプローブ１５１は主にめっきの積み上げにより成形された半球状の金属突起あるいはシリコン基板の異方性エッチング穴をめっき型として形成した角錐状の金属突起などであり、ポリイミドなどの有機薄膜１５２の表面にこの集合体が形成されている。

【０００７】また、後述する上記二例の問題点を解決する手段として、特開平６－１２３７４６号公報、特開平７－７０５２号公報、及び特開平８－５０１４６号公報、特開平９－２４３６６３号公報が公開されている。

【０００８】特開平６－１２３７４６号公報では弾性変形可能なカードに切り込みを入れて個別に弾性変形可能な複数のプローブニードルを均一に形成し、この複数のプローブニードルのそれぞれの先端部に半導体素子の電極に接触可能な複数の接触子を設けている。

【０００９】また、特開平７－７０５２号公報では単結晶シリコン、酸化シリコン、窒化シリコン、ポリシリコン、あるいは金属層の少なくとも一層からなる片持ち梁構造とし、その表面に導通用の金属皮膜を形成した、さらに，この片持ち梁構造体を導通配線パターンを形成した絶縁基板で保持して電気特性測定用プローブとしている。

【００１０】一方、特開平９－２４３６６３号公報ではシリコン基板をダイアフラム状に加工し、コンタクト面に複数のコンタクトプローブを形成した構造のダイアフ

ラム部に、エラストマを充填して電気特性を測定するためのプローブを形成している。

【００１１】

【発明が解決しようとする課題】上記、従来技術で述べたような半導体装置の検査方法では、以下に示すような問題点があった。

【００１２】図１３に示したプローブ構造では、個々のプローブを高精度に位置決め・固定することに多大な時間を必要とし、プローブ構造体を安価に量産することが困難であった。また、個々のプローブを位置決め・固定するための領域を多く必要としたため、基板内により多くのプローブを配置することが困難であり、一回に検査できる電極パッド数あるいはチップ数が限られていた。さらに、個々のプローブ長が数十ｍｍ程度と大きいため、各プローブ内の規制容量が大きく、１００ＭＨｚ程度以上の高速デバイスの検査が実質不可能であった。

【００１３】また、個々のプローブ先端の曲率半径が大きく、被検ウエハの電極パッド表面に形成された絶縁性の自然酸化膜を破壊するために、大きな押圧荷重および電極パッド表面をスクライブ（けがき）する動作を必要とするため、プローブ先端の摩耗を早め、プローブの寿命（耐用検査回数）が短かったばかりか、スクライブにより発生する電極パッドの塵埃が、半導体装置製造における環境を汚染する問題があった。

【００１４】また、図１４に示したプローブ構造では、ポリイミドなどの有機薄膜表面に被検ウエハの電極パッドに対応して微細なピッチでプローブが配置されるため、被検ウエハの反りやプローブの高さのばらつきにより生じるプローブと対応する電極パッドとの距離のばらつきを独立に吸収することが困難であった。また、被検ウエハと大きく線膨張係数の異なるポリイミドなどの有機薄膜を基材としているため、１５０℃程度の高温中で行われるバーンイン検査では、被検ウエハとの間に大きな熱膨張差が生じ、中心から離れた位置にあるプローブでは電極パッドとプローブとの位置ずれが生じる場合があった。

【００１５】また、特開平６－１２３７４６号公報では、カードが合成樹脂あるいは金属で構成されるため、被検ウエハの電極パッド位置に対応した微細なピッチでのプローブ配置、すなわち個々に弾性変形が可能な複数のプローブニードルの形成が困難であった。

【００１６】特開平７－７０５２号公報ではシリコン系基材で形成した個々の片持ち梁プローブを、改めてそれとは別の絶縁基板表面に接合するために製造歩留まりが低下し、さらに個々のプローブの高さが不均一という問題があった。

【００１７】特開平９－２４３６６３号公報では、エラストマ（弾性材）を利用して、被検ウエハの歪みに沿ってシリコン基板内に形成したダイアフラム部が変形すると記載されているが、この方式ではダイアフラムの厚みのばらつきが考慮されておらず、うねりや厚みのばらつきを持ったダイアフラムを変形させた場合、コンタクトプローブの高さの制御ができない。そのため、被検ウエハの電気的特性測定用パッドの深さ方向を制御できないため、押圧力が不足する場合は被検ウエハの電気的特性測定用パッド部に接触しない部分が出てくる。また、押圧力をかけ過ぎた場合は被検ウエハの電気的特性測定用パッド部に深くめり込み、被検ウエハを破壊する問題があった。

【００１８】また、上記のいずれのプローブ構造共、プローブの先端と外部の検査システムとの電気的接続のための配線が、基板中のプローブ形成面と同一表面に形成されるため、すべての外部接続端子を基材の外周近傍に集中して形成せざるを得ず、同外部接続端子の形成可能領域が限定され、多くのプローブを外部と電気的に接続することが困難であり、例えば被検ウエハの全電極パッドを一括して検査するというような大領域同時検査が困難であった。

【００１９】本発明の目的は、これまで述べた多くの問題点を解決し、半導体装置の電気的特性検査において、例えば被検ウエハの全電極パッドを一括検査するというような大領域同時検査を可能とし、それによって製造歩留まりを向上させ、製造コストを低減し、安価で高信頼性を有する半導体装置を得ることにある。

【００２０】

【課題を解決するための手段】上記目的を達成するために、半導体素子と検査装置を直接接触させて、電気的に接続しながら半導体素子を検査する方法において、プローブが形成された基板にプローブが押圧力によって変化することができる梁構造あるいはダイアフラム構造が形成され、検査用半導体素子の電極パッドが形成された被検ウエハを押圧または固定する機構あるいは前記基板のプローブまたはプローブ周辺部を押圧する機構を設けることにより達成できる。また、上記プローブが形成された基板にシリコンを用い、プローブをシリコンまたは金属あるいはそれらの複合材から構成し、絶縁物を介して導電性材料を用いた配線によって、プローブ形成基板の裏面側まで配線されている構造を用いると良い。また、該プローブの先端部に平面部を有することにより、プローブ高さを均一にしかも高精度に形成することが可能である。

【００２１】プローブは個々に独立した両持ち梁に形成された構造が好ましく、プローブを中心面内に形成し、その周囲を卍型形状に梁を形成した構造を用いても良い。これらの梁を含めた構造体の加工には異方性エッチングあるいはドライエッチングを用いる。上記ドライエッチングにはＩＣＰ－ＲＩＥ（Ｉｎｄｕｃｔｉｖｅｌｙ Ｃｏｕｐｌｅｄ Ｐｌａｓｍａ－Ｒｅａｃｔｉｖｅ Ｉｏｎ Ｅｔｃｈｉｎｇ）装置を用いることにより、梁と梁の間隔を狭く形成することが可能で、デバイスの狭ピッ

チ化にも対応することができる。

【００２２】配線は検査ウエハに異方性エッチングあるいはドライエッチングを用いて、該基板を貫通させ、スパッタ、蒸着あるいはめっきを用いて該基板のプローブ形成面とその裏面とを電気的に配線する方法を用いる。また、検査ウエハの貫通孔はドライエッチングを用いて形成する方式が良い。さらに、上記の構造および方法を用いて検査した半導体素子あるいは電子部品は非常に安価で提供することができる。

【００２３】

【発明の実施の形態】以下、図面を用いて本発明の実施例を説明する。図１は本発明による半導体検査装置の検査ウエハの構造の一実地例を示す断面図である。

【００２４】検査ウエハ１１は、両持ち梁又はダイアフラム１２（以後はダイアフラムで説明する）と、プローブ１３と、貫通孔１４とで構成されている。ダイアフラム１２部には、プローブ１３が形成されており、プローブ１３は検査ウエハ１１の底面より数μmから数十μm突き出している。貫通孔１４はプローブ１３と同数個形成されており、検査ウエハ１１の全面は酸化シリコン膜１５で被覆されている。プローブ１３と配線１６は、酸化シリコン膜１５の上に形成してある。配線１６は、個々のプローブ１３からそれぞれの貫通孔１４を経て検査ウエハ１１の反対側面に形成した二次側電極パッド１７まで形成されている。

【００２５】図２は本発明による半導体検査装置の構造の一実施例を示す断面図である。

【００２６】被検ウエハ２１は、図示していない、ＸＹＺθ方向に移動が可能なウエハ固定ステージ２２に真空吸着されている。ウエハ固定ステージ２２は、図１で説明した検査ウエハ１１に形成されたプローブ１３と、被検ウエハ２１に形成された一次側電極パッド２３とを高精度に位置合わせして接続することができる。

【００２７】押圧機構支持基板２４には、検査ウエハ１１に形成された二次側電極パッド１７と外部端子とを電気的に接続するため、弾性構造の一般にポゴピン２５と呼ばれる接続端子と内部配線２６とが形成されている。押圧機構支持基板２４と検査ウエハ１１とは、ポゴピン２５と二次側電極パッド２３とを位置合わせして接続した後に固定される。次に、押圧機構支持基板２４に固定された検査ウエハ１１を、ウエハ固定ステージ２２に吸着した被検ウエハ２１に押し当てる。

【００２８】これにより、一次側電極パッド２３とプローブ１３が接触し、ダイアフラム１２が変形し、一定の荷重がプローブ１３と一次側電極パッド２３間にかかり、全プローブにおいて均一な電気的特性検査が可能になる。なお、ここではウエハ固定ステージ２２にＸＹＺθ方向の移動機構を備えている構成で説明したが、移動機構を押圧機構支持基板２４あるいはウエハ固定ステージ２２と押圧機構支持基板２４の両方に付加しても良い。

【００２９】上記の説明では、ポゴピン２５を用いて検査ウエハ１１に形成された二次側電極パッド１７と外部電極を接続したが、ポゴピン２５の代用としてはんだバンプを用いた構造としても良い。

【００３０】図３は図２で説明した半導体検査装置にさらに押圧機構を付加した構造の断面図である。

【００３１】ポゴピン２５又ははんだバンプだけで、ダイアフラム１２に十分な押圧力が付加されない場合、ダイアフラム１２さらにその他の部位を押圧するためにエラストマ４１、４２を設ける。ただし、エラストマ４１、４２以外の弾性構造体を設けても良い。なお、図２、図３では、検査ウエハ１１の全面を被覆する酸化シリコン膜１５を省略してある。

【００３２】図４は本発明の検査ウエハの加工工程を示す断面図である。

【００３３】（ａ）基板となるシリコンウエハ１１は直径８インチ、厚さ６００μmとし、被検ウエハ２１と同形状のものを使用する方が良い。これにより、製造コストの低減や検査装置の省スペース化を図ることができる。例えば、被検ウエハ２１が直径８インチの場合は、検査ウエハ１１も直径８インチが良い。

【００３４】（ｂ）シリコンウエハ１１の表面に厚さ０．７μmの酸化シリコン膜１５を形成する。その後、フォトリソグラフィ工程によりシリコンエッチング用のパターンを形成する。すなわち、酸化シリコン膜１５の表面にフォトレジストを塗布し、パターンを描いたフォトマスクを用いて露光、現像、エッチングすることにより、酸化シリコン膜１５を部分的に除去し、開口部分を有するパターンを形成する。次に８０℃の３５％水酸化カリウム水溶液で異方性エッチングを行い、酸化シリコンパターンの開口部からシリコンウエハ１１を侵食させて高さ５０μmのプローブ１３を形成する。

【００３５】ここで、シリコンウエハ１１をエッチングするためのパターンに酸化シリコン膜１５を用いたが、代わりに窒化シリコン膜を用いても良い。また、シリコンウエハ１１のエッチング液に水酸化カリウム水溶液を用いたが、それ以外の異方性エッチング液、例えばテトラメチルアンモニウムハイドロオキサイド、エチレンジアミンピロカテコール、ヒドラジン等を用いても良い。

【００３６】（ｃ）酸化シリコン膜パターンを除去し、再度シリコンウエハ１１の全面に酸化シリコン膜１５を１μm形成する。（ｂ）と同様にフォトリソグラフィ工程によりシリコンエッチング用のパターンを形成し、異方性エッチングにより厚さ１００μm、長さ２mmのダイアフラム１２を形成する。

【００３７】（ｄ）酸化シリコン膜パターンを除去し、シリコンウエハ１１の全面に酸化シリコン膜１５を形成する。フォトリソグラフィ工程によりシリコンエッチング用のパターンを形成し、ＲＩＥ（Ｒｅａｃｒｉｖｅ

Ｉｏｎ Ｅｔｃｈｉｎｇ）装置により貫通孔１４を形成する。この時の貫通孔１４は直径１００μｍである。ただし、貫通孔の大きさは個々の半導体チップの大きさの中に電極パッド数分が形成できればこれ以外の大きさでも良い。

【００３８】（ｅ）酸化シリコン膜パターンを除去し、シリコンウエハ１１の全面に酸化シリコン膜１５を０．５μｍ形成する。この酸化シリコン膜１５はプローブ１３と二次側電極パッド１７とをつなぐ配線１６を流れる電流の検査ウエハ内部への漏電を防止するものであるため、これ以外の厚さで形成しても良い。また、酸化シリコン膜ではなく、１５０℃以上で溶融しなければその他の絶縁膜を形成しても良い。

【００３９】（ｆ）フォトリソグラフィ工程により酸化シリコン膜１５の表面にフォトレジストパターンを形成後、シリコンウエハ１１の全面にスパッタリング装置を用いて、まずクロム膜を０．１μｍ形成し、続いてニッケル膜を１μｍ形成する。その後、リフトオフ法を用いてフォトレジストとフォトレジスト上のクロム膜とニッケル膜を除去し、配線１６および二次側電極パッド１７を形成する。

【００４０】配線１６および二次側電極パッド１７の成膜装置はスパッタリング装置に限らず、蒸着装置やＣＶＤ（Ｃｈｅｍｉｃａｌ Ｖａｐｏｒ Ｄｅｐｏｓｉｔｉｏｎ）装置を用いても良い。また、配線１６および二次側電極パッド１７の形成方法はリフトオフ法に限らず、検査ウエハ１１の全面に絶縁膜を形成し、さらに全面に配線用の薄膜を形成後、フォトリソグラフィ工程でエッチングにより形成しても良い。なお、この時のエッチングはエッチング液を用いたウェットエッチングでも、イオンミリング装置などを用いたドライエッチングでもどちらでも良い。さらに、配線材料は１５０℃以上で溶融せず、導電性があり、薄膜形成可能な材料、例えば金、銅、白金、チタン、コバルト、モリブデン、タングステンなどでも良い。

【００４１】図５は本発明によるプローブの形状を示す側面図および平面図である。

【００４２】（ａ）は異方性ウェットエッチングにおいてダイアフラム１２に形成されたプローブ１３である。異方性ウェットエッチングは、アルカリ系エッチング液においてシリコンの結晶面の違いによってエッチング速度が異なることを利用した加工方法である。このため、（１００）面のシリコンウエハの場合、（１００）面と（１１１）面で囲まれた角錐状のプローブ１３が形成される。

【００４３】（ｂ）は（ａ）よりさらにエッチングが進行した状態のプローブを示したものである。（１００）面と（１００）面及び（１００）面と（１１１）面が互いに交叉する稜には（１００）面および（１１１）面以外にも多くの結晶面が現れている。このため、（１１０）面や（３１１）面などの（１００）面や（１１１）面よりエッチレートの速い結晶面が現れるような形状になる。

【００４４】（ｃ）はＲＩＥ装置などのドライエッチングにより円柱状に突起を形成した後、ダイアフラム１２の表面および円柱の先端部に酸化シリコンなどのマスクパターンを形成し、シリコンウエハを傾斜させてさらにイオンミリング装置などでドライエッチングを行い円錐状に形成したプローブである。このとき、傾斜させたシリコンウエハは自転および公転させながらドライエッチングを行った方が良い。

【００４５】（ｄ）はＲＩＥ装置などのドライエッチングにより先端部と同じ径の円柱状に形成したプローブである。（ｅ）および（ｆ）は異方性ウェットエッチングとドライエッチングとの複合エッチングによるプローブである。（ｅ）は（ａ）と（ｄ）の組み合わせ、（ｆ）は（ｃ）と（ｄ）の組み合わせである。このように、プローブ１３の形状に特に制限はないが、プローブ１３の高さが決まっているとき（ａ）から（ｃ）の方法ではプローブ１３の先端部面積と比較してダイアフラム１２に接するプローブ１３の面積が大きいため、プローブ間ピッチをあまり狭くできない。

【００４６】プローブ間ピッチが狭い場合は（ｄ）から（ｆ）のような形状が良いが、強度的には（ａ）から（ｃ）の形状より劣る。従って、プローブ１３の形状は一次側電極パッドのピッチ、押圧力、梁又はダイアフラムのたわみ量、プローブ高さなどを考慮しながら決定する方が良い。

【００４７】一方、（ａ）から（ｆ）のプローブ１３には先端の一次側電極と接触する部分に、プローブ１３の形成時にエッチングしない平坦部を形成しておくと良い。異方性ウェットエッチングによりプローブ１３の先端に平坦部を設けずに尖った形状を形成すると、尖った瞬間にマスクが消滅してしまう。異方性ウェットエッチングとはいえ、エッチング液温などを精密に管理しない限り、シリコンウエハ内では数％のエッチングによるばらつきが生じるため、プローブ１３の先端部の高さが不均一になってしまう。

【００４８】しかしながら、プローブ１３の先端に平坦部を形成すると、プローブ１３の高さは均一になる。このため、被検ウエハ２１の一次側電極パッド２３と検査ウエハ１１のプローブ１３を接続した場合に、検査ウエハ１１の全てのダイアフラム１２の変位量が一定になる。従って、検査ウエハ１１の全てのプローブ１３の荷重が一定になるため、被検ウエハ２１の全ての一次側電極パッド２３に対して均一で高精度な検査が可能になる。なお、プローブ１３の先端の平坦部６１の形状は四角形、円形に限らず、その他の多角形でも良い。

【００４９】図６は半導体チップに形成される一次側電極パッドの配列である。

【００５０】パッド配列には（ａ）主にＤＲＡＭ（読取専用記憶素子）のように半導体チップ７１の中心線に沿って電極パッド７２がほぼ一直線状に並んだものと、（ｂ）主にマイコンのように半導体チップ７３の周辺部に電極パッド７４が直線状に並んだものとに大別できる。（ａ）および（ｂ）とも個々の電極パッド７２、７３の寸法は数十μｍ角から数百μｍ角であり、パッド間ピッチも数十μｍから数百μｍである。

【００５１】図７は本発明による梁あるいはダイアフラムの構造を示す平面図である。

【００５２】（ａ）（ｂ）（ｃ）は中心部に一直線状に並んだ半導体チップ用である。（ａ）は本発明による両持ち梁構造である。検査ウエハ１１に形成された両持ち梁１２のそれぞれに対してプローブ１３が一個ずつ形成されている。プローブ間ピッチは、一次側電極パッド間ピッチに対向させるが、梁幅、梁長、梁厚は全てのプローブで同寸法とし、プローブにかかる荷重を一定にする。

【００５３】（ｂ）は本発明によるダイアフラム構造である。プローブ１３の並ぶ方向にスリット８１を形成し、ダイアフラム１２のたわみ量を均一にして個々のプローブ１３にかかる荷重を一定にしている。一次側電極のパッド間ピッチが狭い場合や、両持ち梁構造と同スペースでプローブ荷重を増大させたい場合に有効である。

【００５４】（ｃ）は四方向にスリット８１を設けた構造である。一次側電極のパッド間ピッチが狭く両持ち梁は形成できないがプローブ荷重は減少させたい場合に有効である。（ｄ）（ｅ）（ｆ）は周辺部に直線状に並んだ半導体チップ用であり、（ｄ）は（ａ）の、（ｅ）は（ｂ）の、（ｆ）は（ｃ）の応用例である。特に（ｆ）はプローブ１３が配置された中心部と周辺部とを接続する両持ち梁１２を卍型に形成し、プローブ１３の変位量を増大させる構造になっている。卍型に限らず、例えば、渦巻型など梁長を長くするような構造にすればプローブの変位量をさらに増大させることができる。

【００５５】図８は本発明による両持ち梁の構造を示す断面図と平面図である。

【００５６】ＲＩＥ装置などを用いたドライエッチングあるいは弗酸－硝酸－酢酸の混合液などを用いた等方性エッチングにより、両持ち梁１２の付け根部分９１、９２に丸みを形成することで、両持ち梁１２の剛性および耐久性を増大させ、繰り返し検査における信頼性を向上させることができる。丸みを形成することは両持ち梁に限らず、ダイアフラムや片持ち梁においても有効な手段である。

【００５７】図９はエッチング方法による貫通孔の形状を示す平面図と断面図である。（ａ）（ｂ）（ｃ）のいずれもＸ＝２ｍｍ、Ｙ＝２ｍｍ、Ｚ＝６００μｍの（１００）面のシリコンウエハにｄ＝１００μｍの貫通孔を形成するものとし、貫通孔が互いに重ならないようにＬ＝１００μｍの間隔を開けて並ぶように形成する。

【００５８】（ａ）は異方性ウェットエッチングによって、シリコンウエハ１０１の片側から貫通孔１０２を形成したものである。異方性ウェットエッチングにおいては約５４．７°の斜面を持つ４つの（１１１）面１０３に囲まれた逆四角錐状の貫通孔１０２が形成される。この時、Ｄ１＝２Ｚ／ｔａｎ５４．７°＋ｄ＝９４９μｍ、Ｐ１＝Ｄ１＋Ｌ＝１０４９μｍとなり、□２ｍｍのシリコンウエハ１０１には４個の貫通孔１０２しか形成できない。

【００５９】（ｂ）は異方性ウェットエッチングによってシリコンウエハ１０１の両側から貫通孔１０４を形成したもので、逆四角錐状の貫通孔をつなぎ合せた鼓状の形状をしている。この時、Ｄ２＝Ｚ／ｔａｎ５４．７°＋ｄ＝５２４μｍ、Ｐ２＝Ｄ２＋Ｌ＝６２４μｍとなり、□２ｍｍのシリコンウエハ１０１には９個の貫通孔１０４形成できる。

【００６０】（ａ）、（ｂ）とも貫通孔１０２、１０４のｄの寸法を小さくしたところで□２ｍｍのシリコンウエハ１０１に形成できる数量に変化はなく、異方性ウェットエッチングにおける加工限界がある。

【００６１】一方、（ｃ）はＲＩＥ装置などのドライエッチングによってシリコンウエハ１０１に貫通孔１０５を形成したものである。ドライエッチングのために貫通孔１０５はマスクパターンとほぼ同形状のほぼ垂直な形状になる。このため、Ｄ３＝ｄ＝１００μｍ、Ｐ３＝Ｄ３＋Ｌ＝２００μｍとなり、□２ｍｍのシリコンウエハ１０１には１００個の貫通孔１０５が形成されることになる。

【００６２】また、ＲＩＥ装置の加工限界をアスペクト比（加工深さ／加工幅）で表すことがある。特にＩＣＰ－ＲＩＥ装置の場合のアスペクト比は、１５から２０といわれている。厚さ６００μｍのシリコンウエハ１０１を片側から加工する場合は、貫通孔１０５の最小加工寸法は３０μｍから４０μｍとなる。さらに、両側から加工する場合は、貫通孔１０５の最小加工寸法は１５μｍから２０μｍとなる。そのため、□２ｍｍのシリコンウエハ１０１には数千個形成できる。従って、個々の半導体チップの真上に、それぞれの半導体チップに形成された電極パッドと同数の貫通孔を形成することができる。これにより配線を短くでき、配線抵抗も低減できる。

【００６３】図１０は本発明による被検ウエハと検査ウエハの全体概要を示す斜視図である。被検ウエハ２１には半導体チップ１１１が数百個形成されており、それぞれの半導体チップ１１１には電極パッド２３が数十個から百数十個形成されている。また、検査ウエハ１１には両持ち梁あるいはダイアフラム１２が被検ウエハ２１の半導体チップ１１１と同数あるいはそれ以上形成されており、それぞれの両持ち梁あるいはダイアフラム１２には半導体チップ１１１に形成された電極パッド２３に対

向してプローブが形成されている。さらに、検査ウエハ１１にはそれぞれの両持ち梁あるいはダイアフラム１２の周辺に貫通孔１４が形成され、個々のプローブからの配線が貫通孔１４から取り出される。

【００６４】図１１は本発明によるバーンイン検査用パックの構造を示す断面図である。検査ウエハ１１には変形が容易な両持ち梁１２またはダイアフラム１２が形成され、両持ち梁１２あるいはダイアフラム１２にはプローブ１３が形成されている。検査ウエハは図５で説明した加工工程を経て被検ウエハと同サイズあるいはそれ以下のサイズに形成する。また、例えば、径８インチの被検ウエハに対して径６インチの検査ウエハを切断して組み合せ、径８インチの被検ウエハを一括検査することも可能である。これは歩留まりなどを考慮したもので、例えば、検査ウエハの一部が破損した場合でも容易に交換することで製造コストを低減することが可能である。

【００６５】また、バーンイン検査では１５０℃前後という高温で長時間の電気的測定を行うため、被検ウエハ２１と同じ材質であるシリコンを検査ウエハ１１に用いることで、熱膨張によるプローブの位置ずれなども発生しない。被検ウエハ２１はウエハ固定ステージ２２に真空チャックで固定されている。また、検査ウエハ１１は押圧機構支持基板２４に固定される。ウエハ固定ステージ２２はＸＹＺθ方向に移動が可能であり、これにより被検ウエハ２１と検査ウエハ１１は高精度に位置合わせできる。位置合わせ後、全体をバーンイン検査用パック１２１で固定する。バーンイン検査用パック１２１の材質は、１５０℃以上で熱変形が小さく、窒化アルミニウムやインバーなどのシリコンとの熱膨張係数差が小さいものが良い。

【００６６】但し、バーンイン検査用パック１２１には、被検ウエハ２１に形成された電極パッド２３と検査ウエハ１１に形成されたプローブ１３との電気的測定用の配線２６を取り出すための端子１２２が形成されている。一般にバーンイン検査においては、被検ウエハに形成された数百個のチップに形成された数万個の電極パッドの全てに検査ウエハに形成されたプローブを接続させる必要があるが、本発明のバーンイン検査用パックを用いることにより電気的測定が容易にできる。

【００６７】図１２は本発明によるバーンイン検査用パックの周辺装置の概略を示す断面図である。バーンイン検査装置１３１の中には恒温槽１３２があり、恒温槽１３２の中にバーンイン検査用パック１２１が複数個配置されている。恒温槽１３２の温度管理は温度制御装置１３３により制御されている。バーンイン検査用パック１２１には数万本の配線１３４がつながっており、高速スイッチング回路１３５を介して、テスタ回路１３６に接続されている。高速スイッチング回路１３５は配線１３４を切替えるためのもので、テスタ回路１３６の入力配線数を減少することができる。

【００６８】また、前記高速スイッチング回路１３５はシリコン製であるため、バーンイン検査用パック１２１の中の検査ウエハ１１に高速スイッチング回路を作り込み、バーンイン検査用パック１２１からの配線を大幅に減少させた構造とすることもできる。

【００６９】このバーンイン検査用パックの技術は、プロービング検査装置にも適用することが可能である。このため、ウエハレベルで検査することができ、検査時間の短縮化によるコスト低減が図れる。また、検査ウエハ１１に形成される被検ウエハ２１に形成された個々の半導体チップ１１１と同数だけ形成するだけでなく、それ以上でも良い。これにより、検査ウエハ１１に形成されたプローブ１３が寿命などにより使用できなくなった場合でも、検査ウエハ１１と被検ウエハ２１の位置を変えるだけで、再び被検ウエハ一括検査が可能になる。

【００７０】以上のような本発明をプロービング検査装置およびバーンイン検査装置に適用し、検査ウエハの配線１６の接触抵抗が０．５Ω以下、テスト周波数２００ＭＨｚ以上という結果が得られた。また、その時のプローブ１３の寿命は３０万回以上であった。また、本発明は被検ウエハの電極パッドの検査を確実に行うことが可能であるため、ＬＳＩ用の電極および微細パターン引き出し用あるいは接続用のコネクタなどに用いることができる。さらに、本発明ではプローブ形成基板にシリコンを用いているため、前記プローブ形成基板加工時に抵抗あるいは回路などを組み込みまたは形成することが可能である。

【００７１】

【発明の効果】本発明によれば、半導体装置製造工程の一工程である電気的特性検査工程において、被検体の電極パッドの大領域一括検査が可能となる。

【図面の簡単な説明】

【図１】本発明の一実施例に関する検査ウエハの断面図である。

【図２】本発明の一実施例に関する検査体構造の断面図である。

【図３】本発明の他の一実施例に関する検査体構造の断面図である。

【図４】本発明の一実施例に関する検査ウエハ加工工程の断面図である。

【図５】本発明の一実施例に関するプローブの側面図および平面図である。

【図６】半導体チップの電極パッドの配列を示す平面図である。

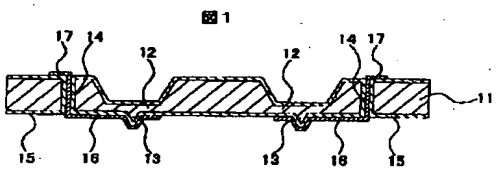
【図７】本発明の一実施例に関する梁およびダイアフラムを示す平面図である。

【図８】本発明の一実施例に関する断面図および平面図である。

【図９】本発明の一実施例に関する平面図および断面図である。

【図１０】本発明の一実施例に関する斜視図である。
【図１１】本発明の一実施例に関する断面図である。
【図１２】本発明の一実施例に関する断面図である。
【図１３】従来技術に関する断面図である。
【図１４】他の従来技術に関する断面図である。
【符号の明】
１１…検査ウエハ、１２…両持ち梁あるいはダイアフラム、１３…プローブ、１４…貫通孔、１５…絶縁膜、１６…配線、１７…二次側電極パッド、２１…被検ウエハ、２２…ウエハ固定ステージ、２３…一次側電極パッド、２４…押圧機構支持基板、２５…ポゴピン、２６…内部配線、３１…はんだボール、４１、４２…エラストマ、６１…平坦部、７１…半導体チップ、７２…電極パッド、７３…半導体チップ、７４…電極パッド、８１…スリット、９１、９２…丸み、１０１…シリコンウエハ、１０２…貫通孔、１０３…（１１１）面、１０５…貫通孔、１１１…半導体素子、１２１…バーンイン検査用パック、１２２…端子、１３１…バーンイン検査装置、１３２…恒温槽、１３３…温度制御装置、１３４…配線、１３５…高速スイッチング回路、１３６…テスタ回路、Ｘ…シリコンウエハの横寸法、Ｙ…シリコンウエハの縦寸法、Ｚ…シリコンウエハの高さ寸法、Ｐ１、Ｐ２、Ｐ３…貫通孔間ピッチ、ｄ、Ｄ１、Ｄ２、Ｄ３…貫通孔開口幅、Ｌ…貫通孔間隔。

【図１】



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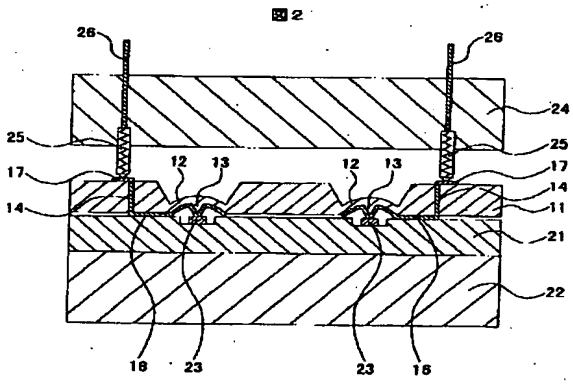

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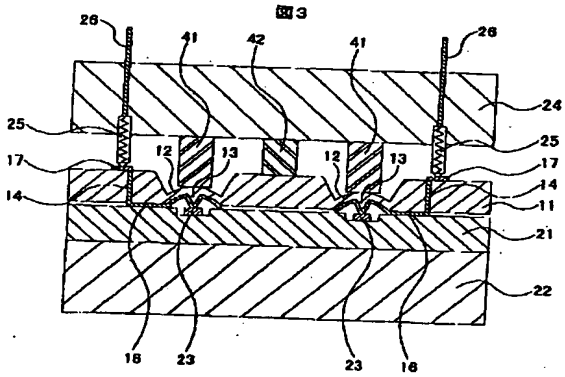

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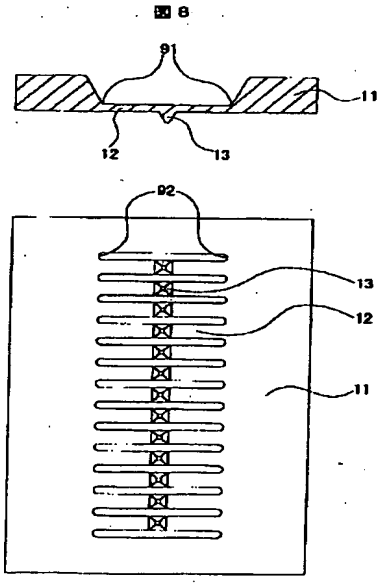
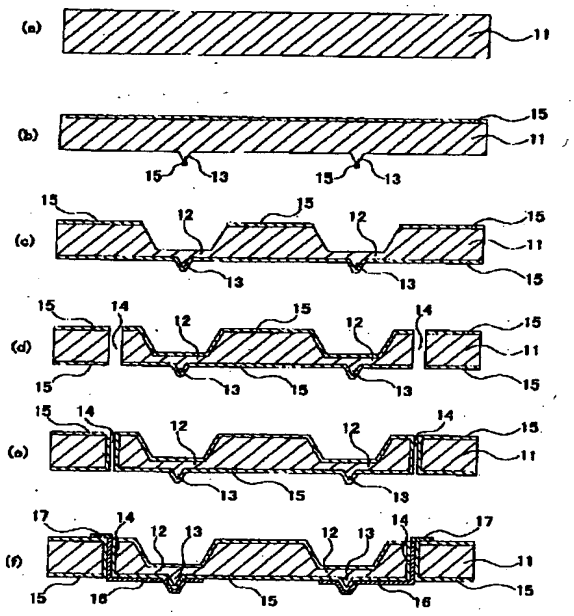


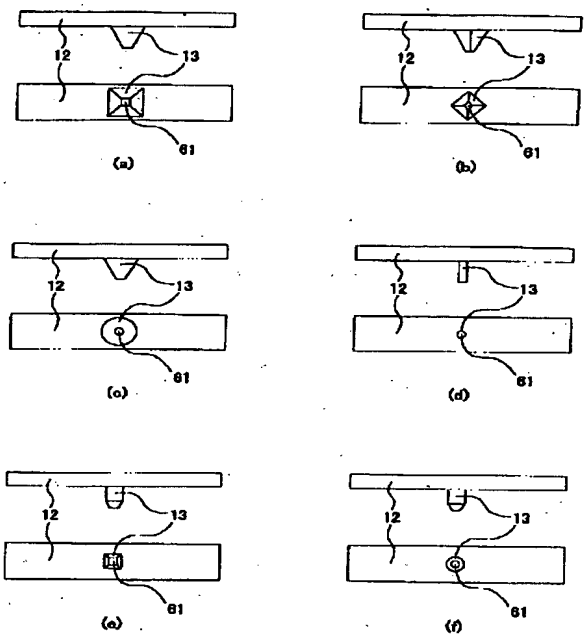
【図４】

図４



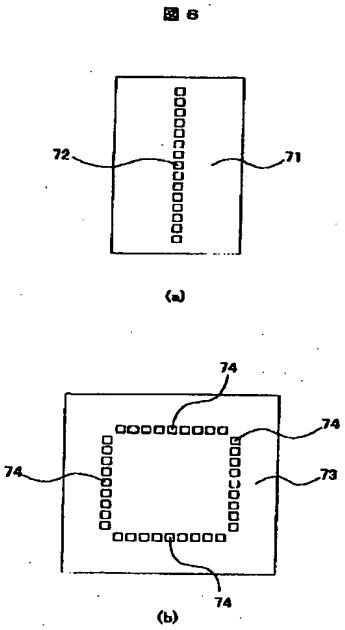
【図５】

図５



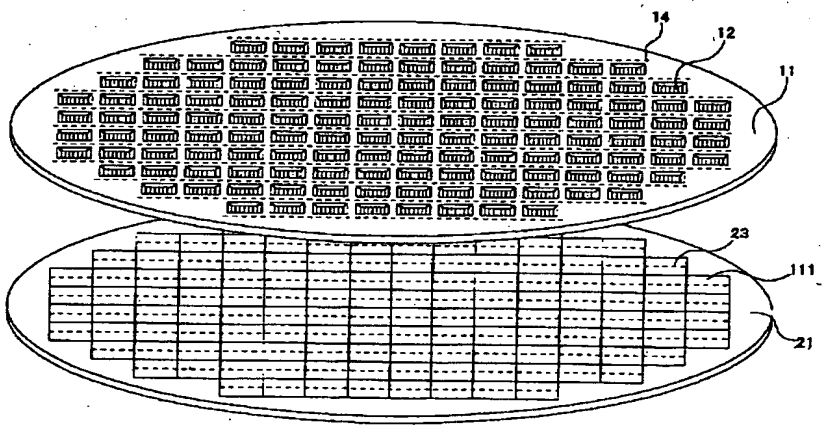
【図６】

図６



【図１０】

図１０



【図７】

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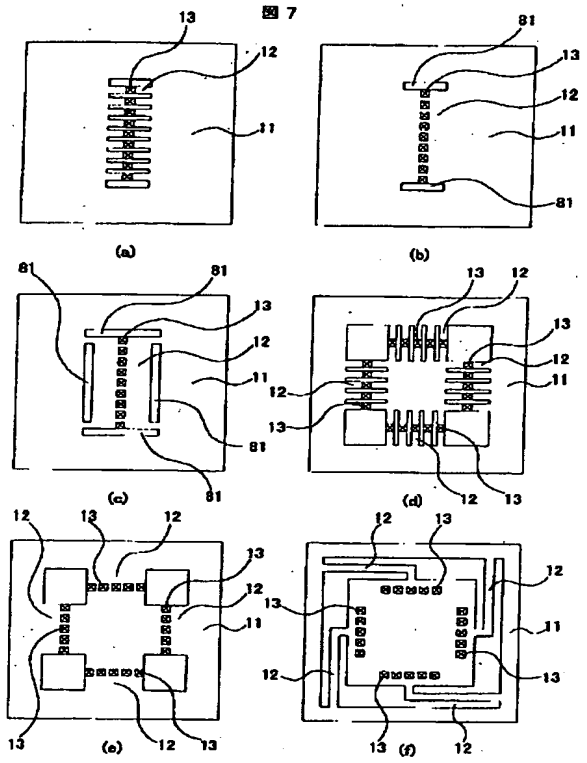
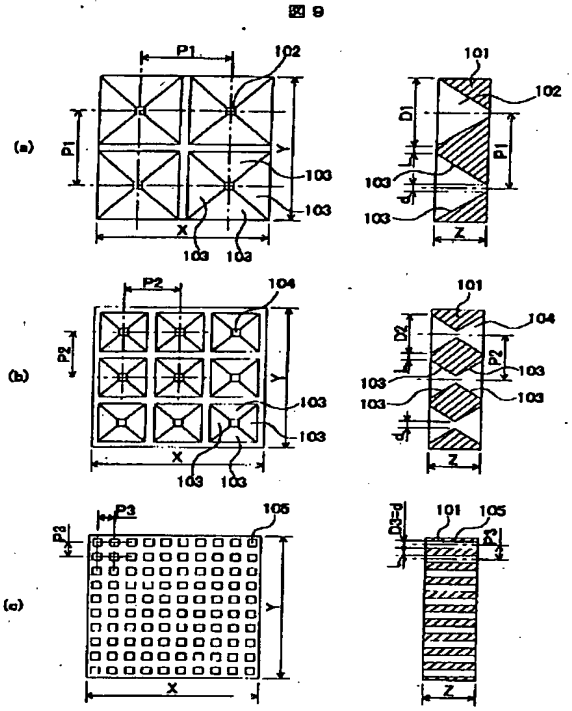


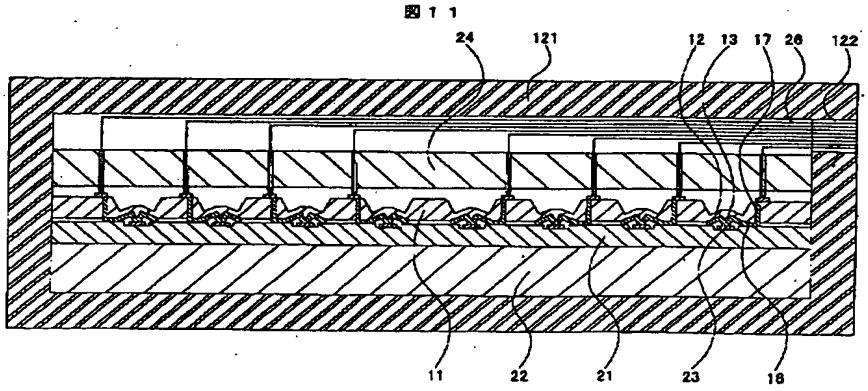
【図９】

図９



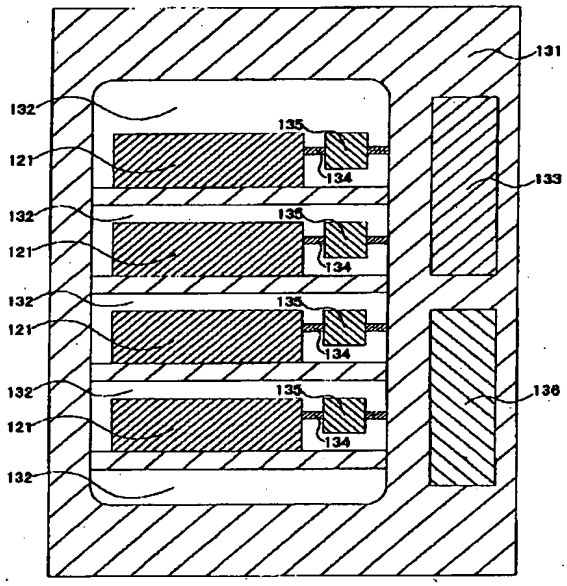
【図１１】

図１１



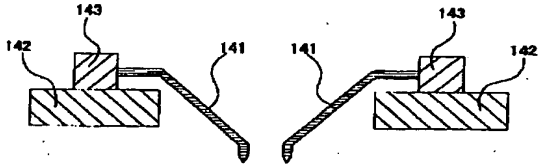
【図１２】

図１２



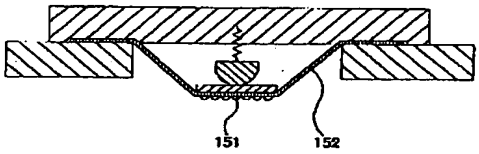
【図１３】

図１３



【図１４】

図１４



フロントページの続き

(72)発明者　河野　竜治
茨城県土浦市神立町502番地　株式会社日立製作所機械研究所内
(72)発明者　遠藤　喜重
茨城県土浦市神立町502番地　株式会社日立製作所機械研究所内
(72)発明者　有賀　昭彦
東京都小平市上水本町五丁目20番１号　株式会社日立製作所半導体事業部内
(72)発明者　伴　直人
東京都小平市上水本町五丁目20番１号　株式会社日立製作所半導体事業部内
(72)発明者　青木　英之
東京都小平市上水本町五丁目20番１号　株式会社日立製作所半導体事業部内

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